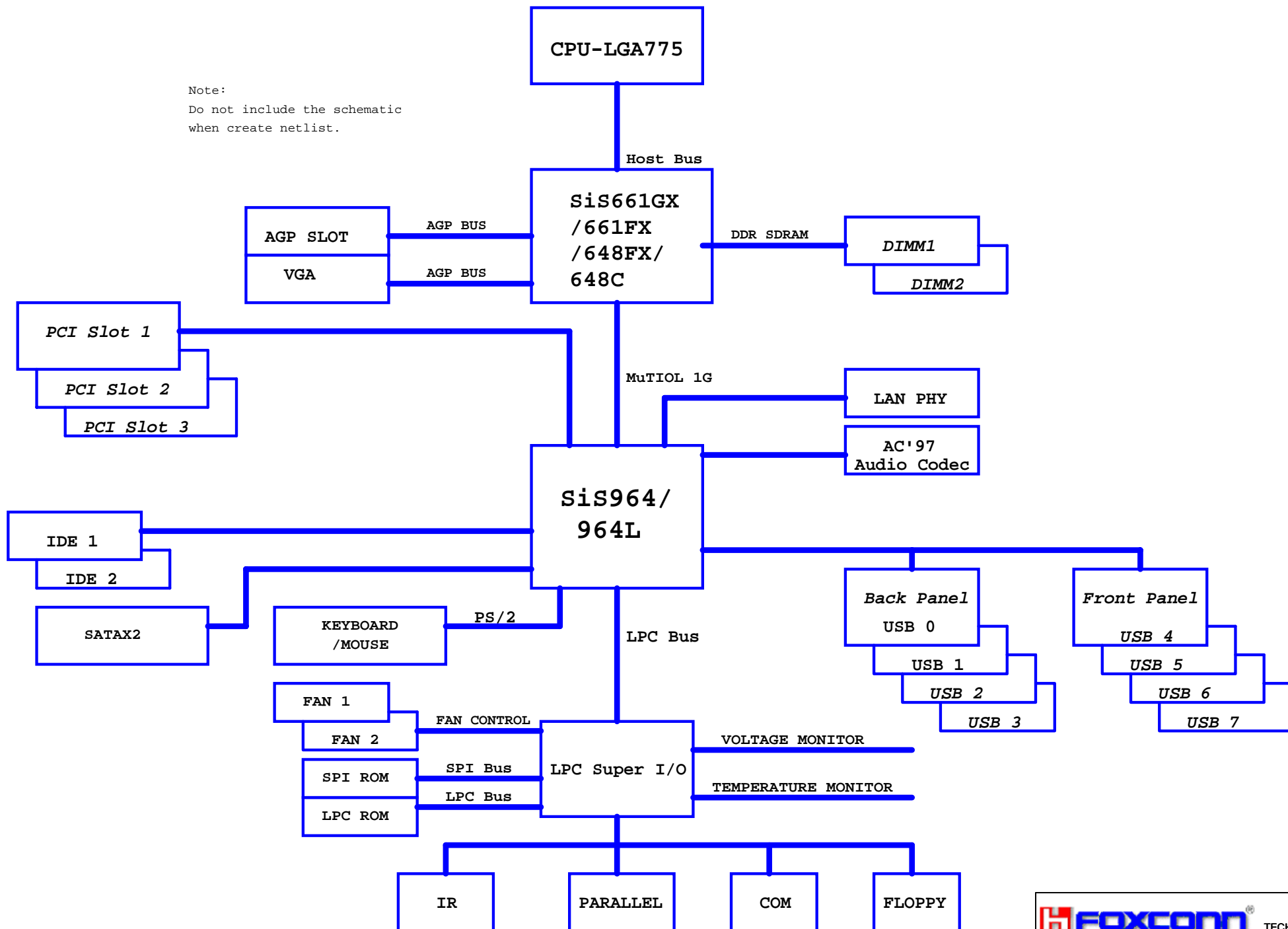


Note:  
Do not include the schematic  
when create netlist.



# Foxconn Precision Co. Inc.

## 661M08 Schematic

Fab.A

Data: 2005/06/28

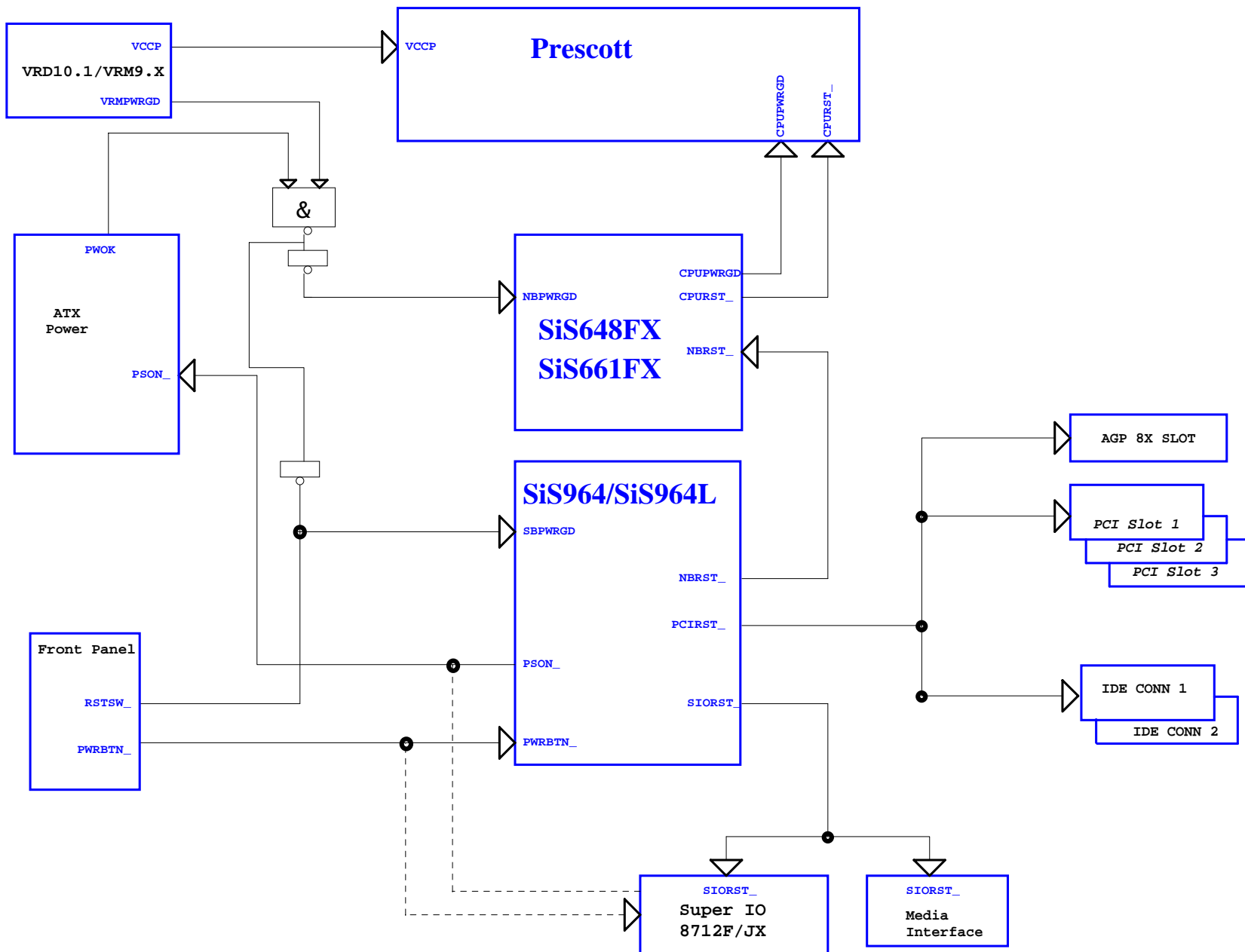
### Page Index

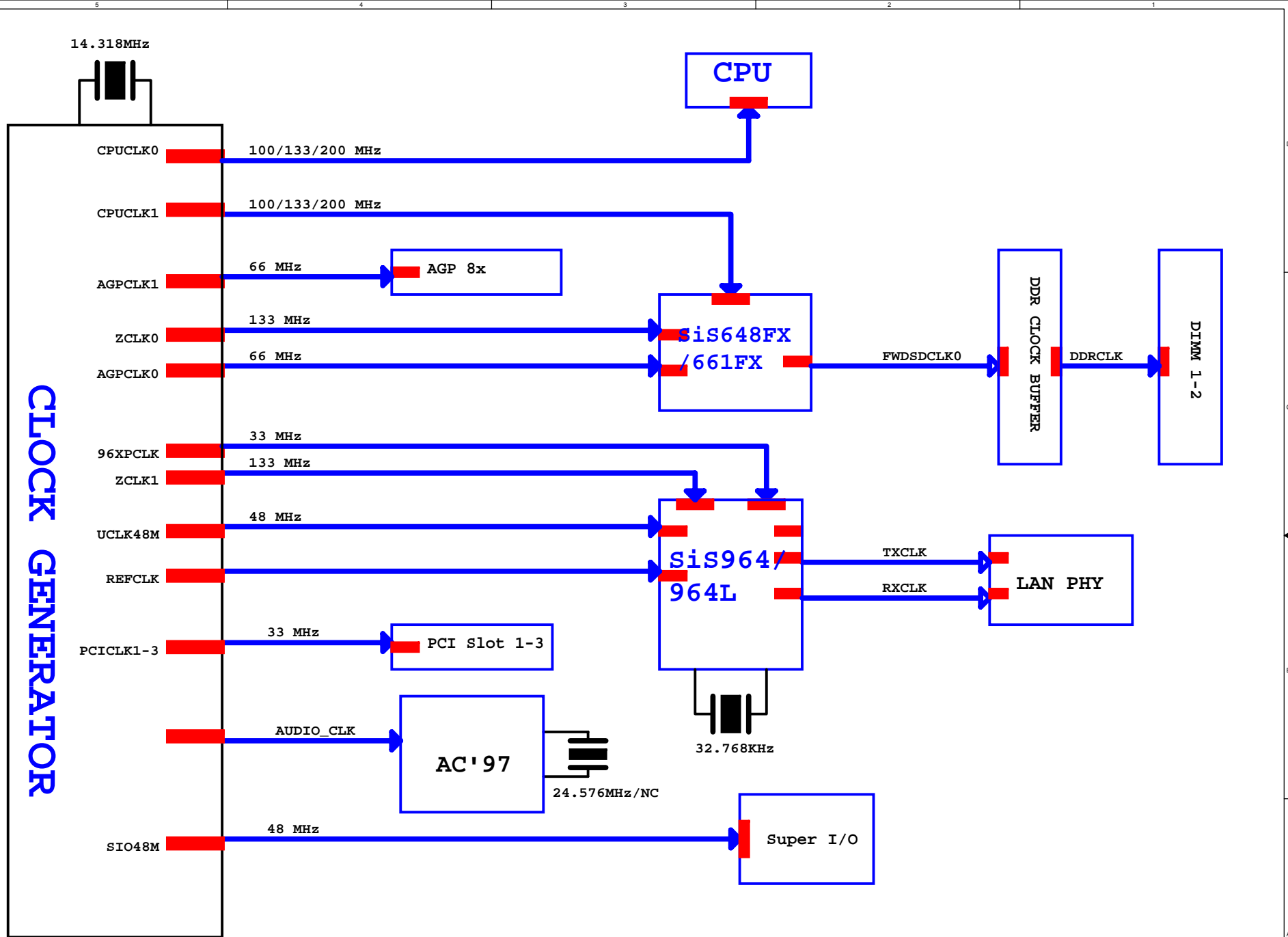
00. Index Page	22. DECOUPLE & EMI
01. Topology	23. Termination
02. Rest Map	24. PCI 1&2
03. Clock Distribution	25. PCI3
04. Power Delivery Map	26. IDE CONN
05. LGA775-1	27. USB & LAN PORT
06. LGA775-2	28. SI/O_ITE8712F/JX
07. Voltage regulator Down 10.1	29. K/B & MS CONN
08. Output CAP	30. COM/PRT/GAME PORT
09. 661FX-1 HOST & AGP	31. LPC/SPI BIOS_FLOPPY
10. 661FX-2 DDR	32. FAN
11. 661FX Mutiol & VGA	33. 653/655 AC97 CODEC
12. 661FX Power	34. AC97 I/O
13. 964/L-1 PCI/IDE/Link	35. LAN PHY AC131KML
14. 964/L-2 PC/MIL/CPU/GPIO	36. Power BTN/RTC Batt
15. 964-3 USB/SATA	37. DDR 2.5V DDRVTT
16. 964-4 Power	38. Power CONN
17. 952017/18AF Clock GEN	39. SB3V, SB1.8V, VCC1.8V, VDDQ
18. DDR Clock Buffer	40. TI1394(NA)
19. AGP	41. USB
20. VGA CON	42. Modification
21. DIMM1 & DIMM2	43. Jumper Setting/Option Table

**FOXCONN®**

**FOXCONN PCEG**

Title <b>Index Page</b>		
Size B	Document Number <b>661M08</b>	Rev A
Date: Monday, August 01, 2005	Sheet 1	of 44

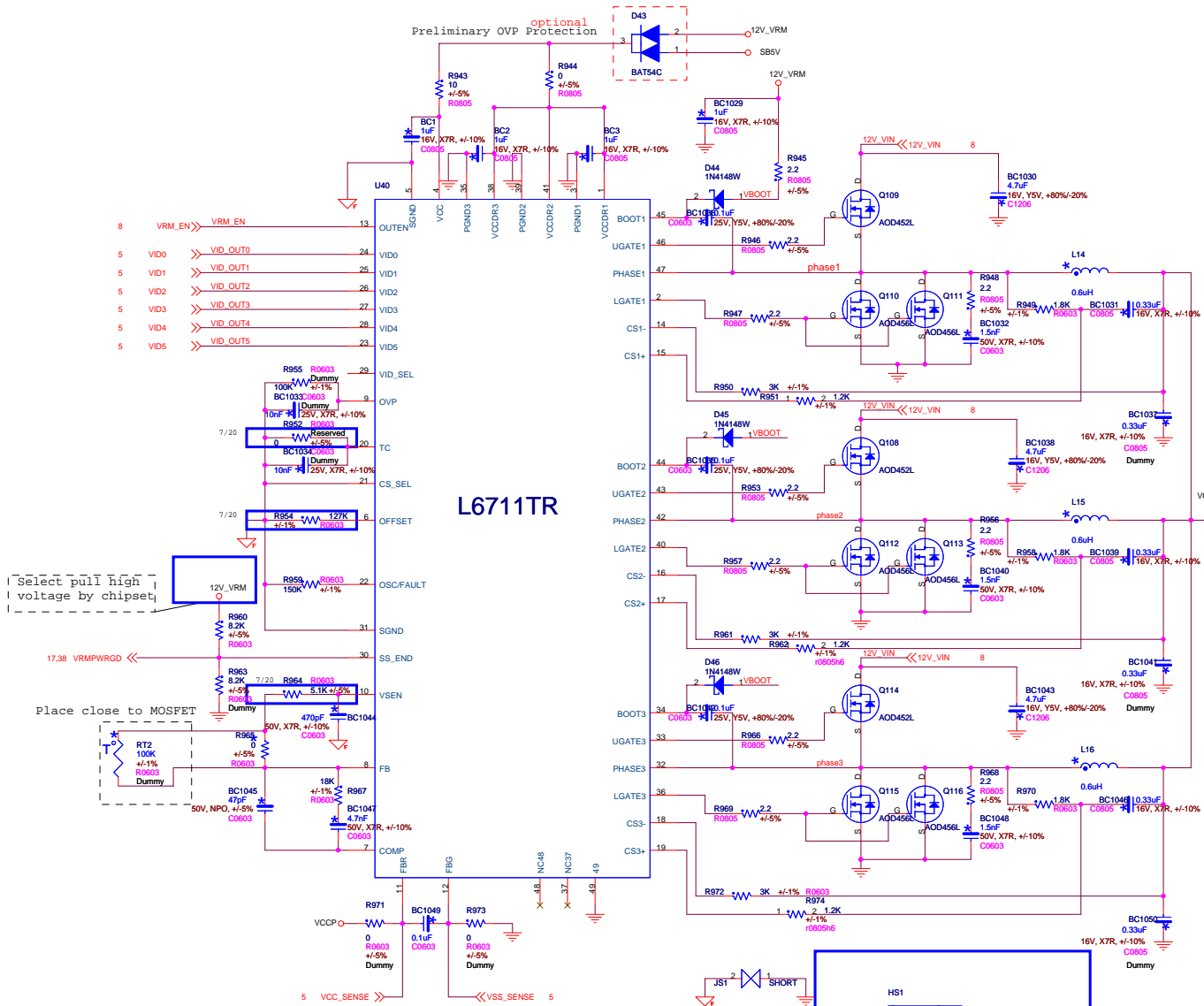






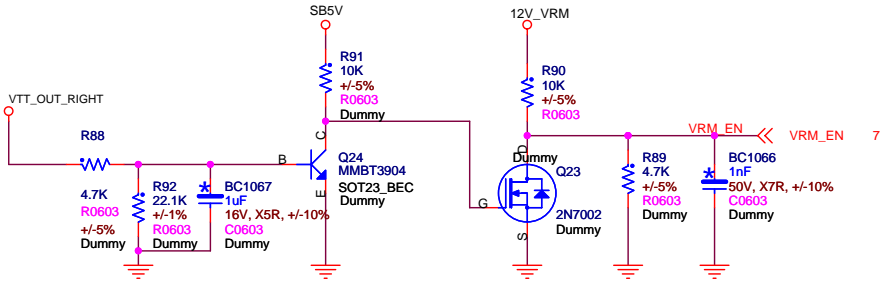




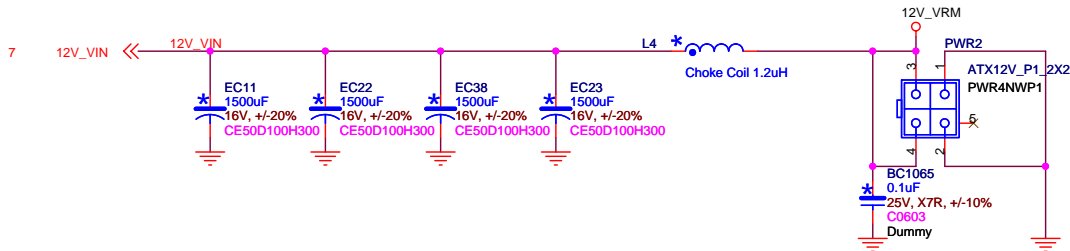




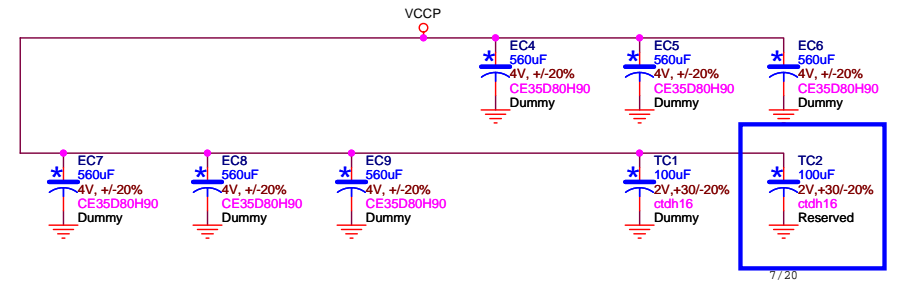
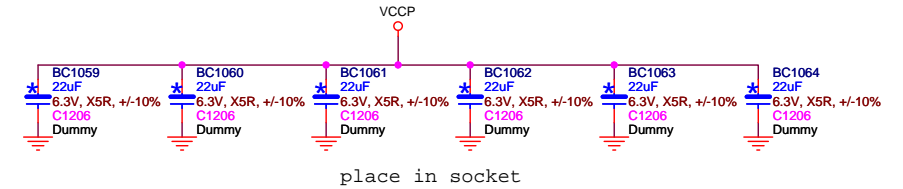
## PWM Controller Enable schematics



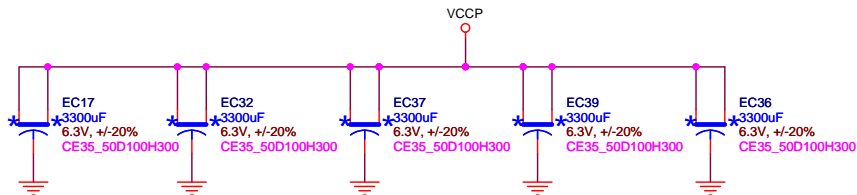
## VRM Input LC schematics

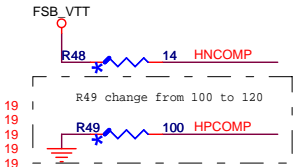
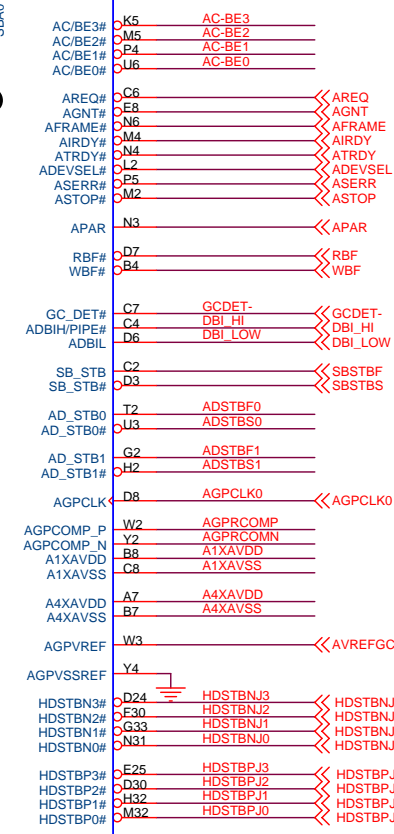
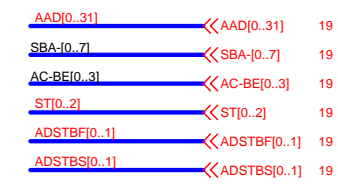
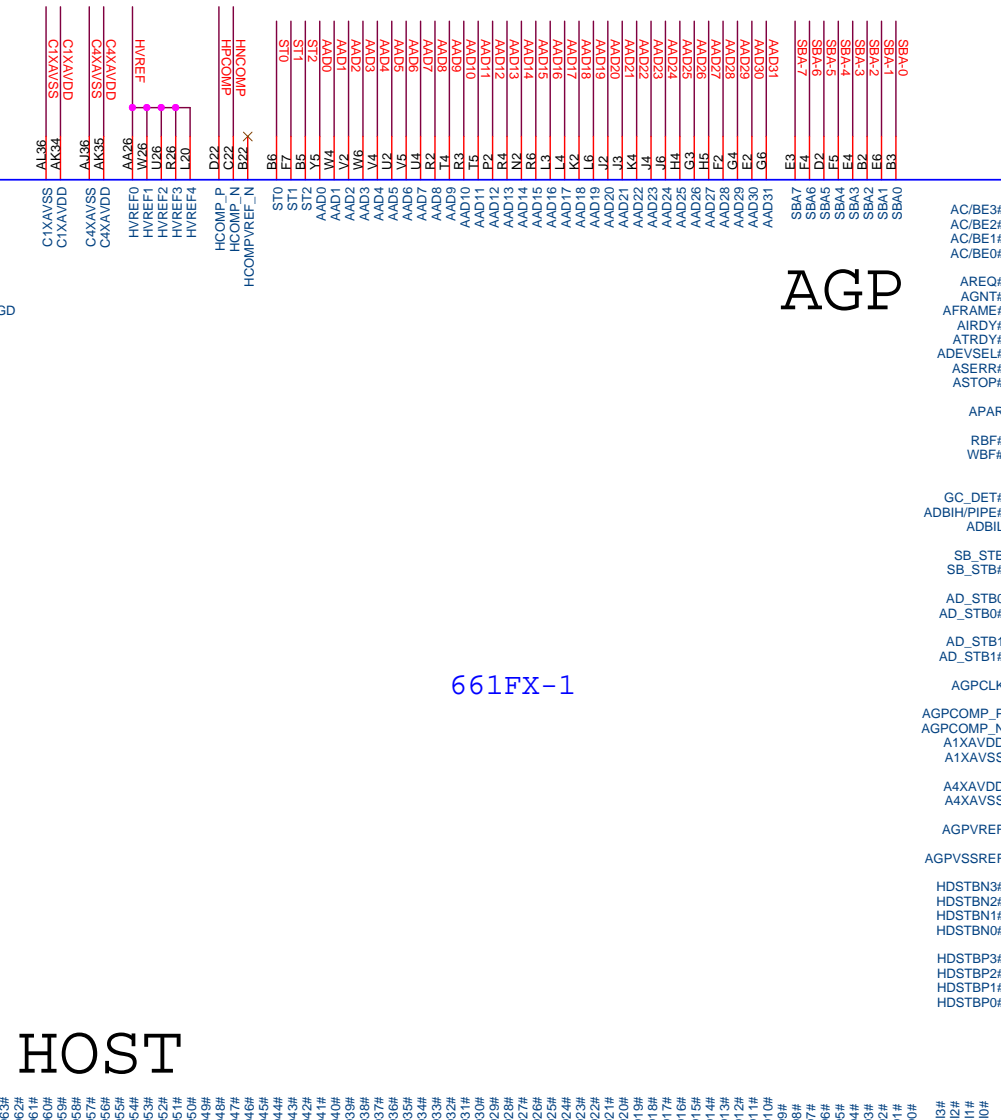
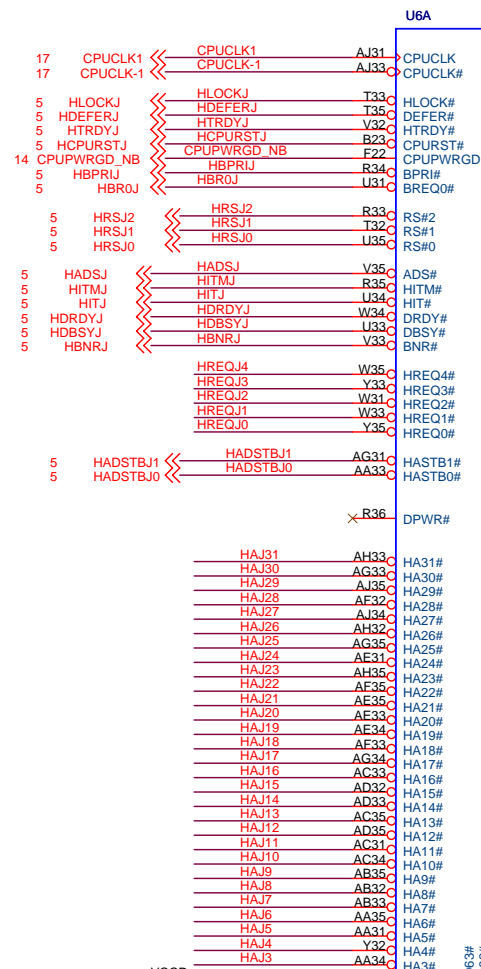
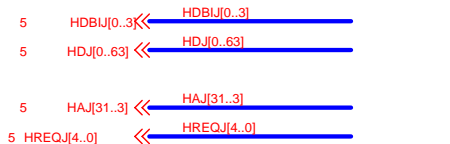


## VRM Output MLCC

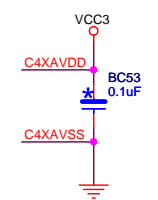
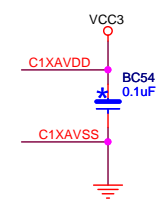
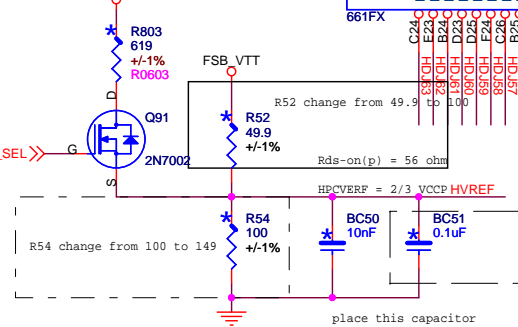
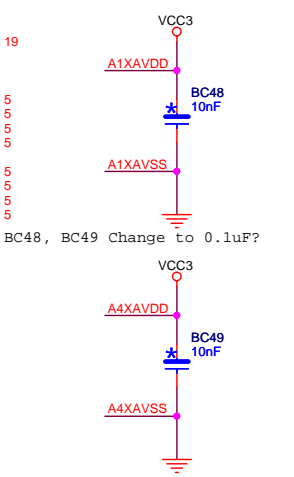
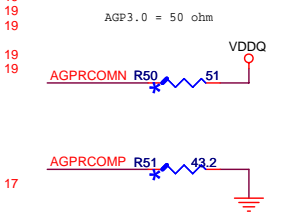


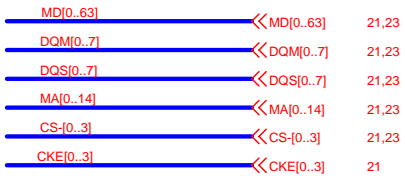
## VRM Output filter schematics





	R48	R49
648	10 1%	113 1%
648FX	14 1%	100 1%
661FX	14 1%	100 1%



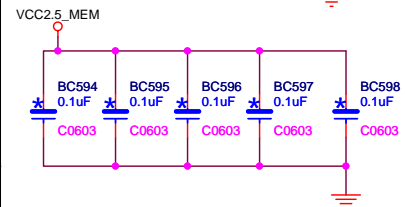
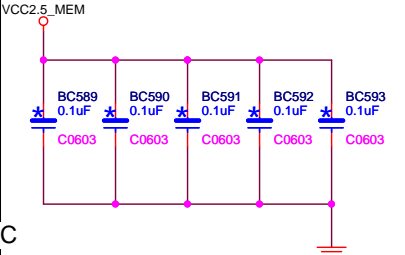


D

C

B

A

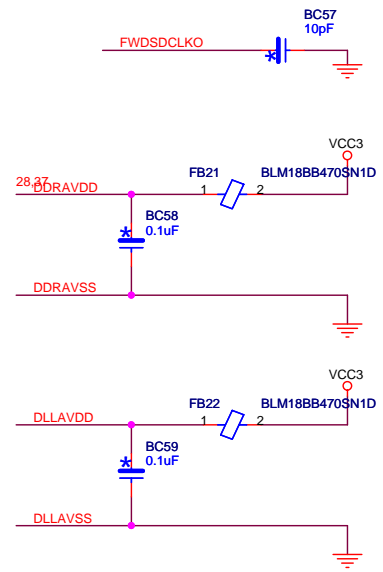
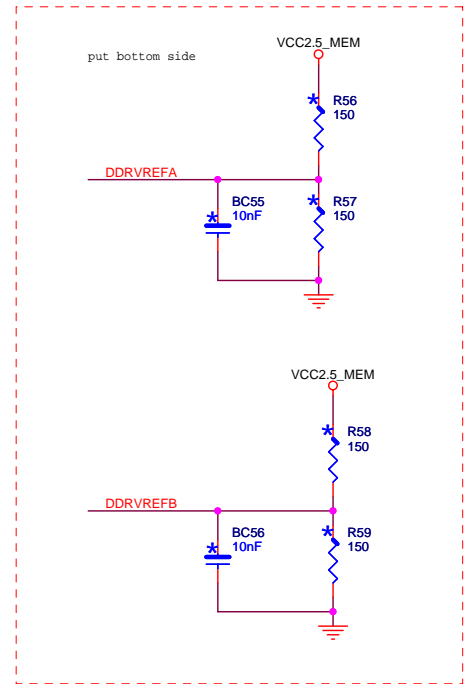
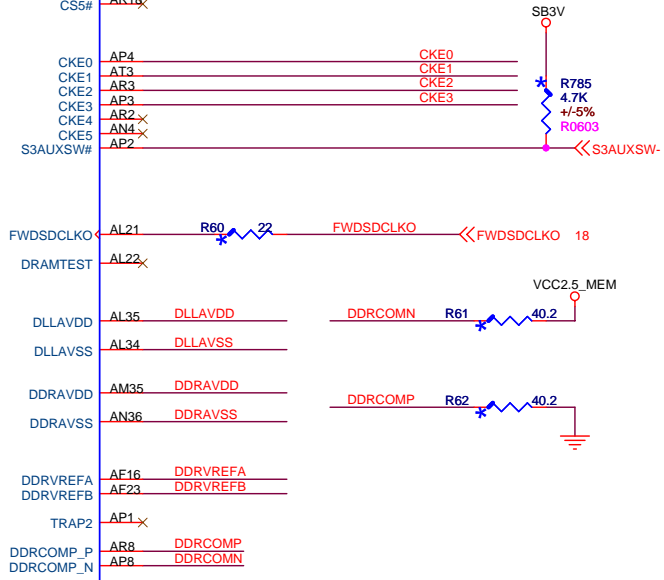


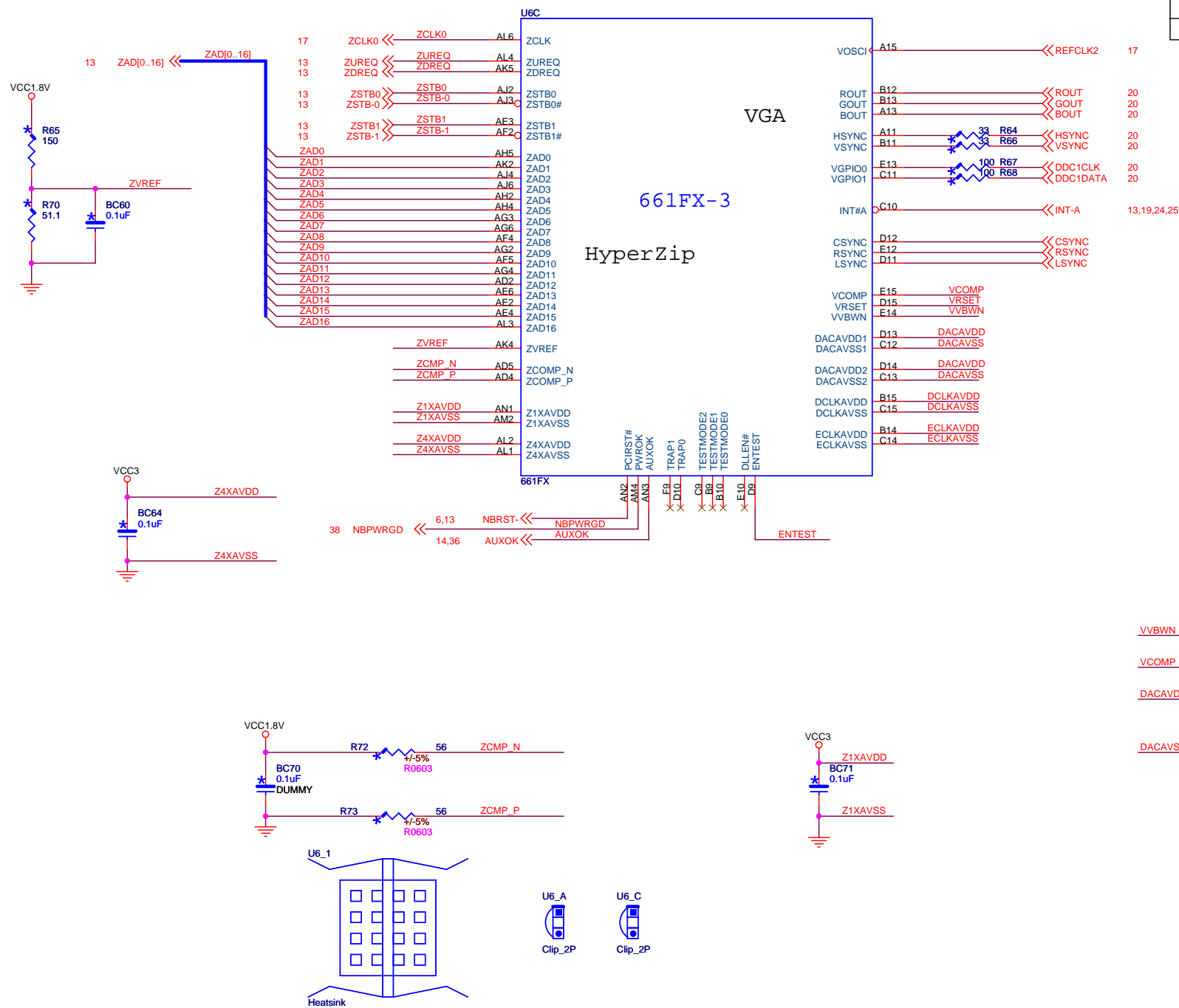
U6B		
MD0	AN35	MD0
MD1	AP36	MD1
MD2	AK33	MD2
MD3	AM33	MD3
MD4	AN34	MD4
MD5	AK32	MD5
MD6	AR34	MD6
MD7	AN33	MD7
DQM0	AR35	DQM0
DQS0	AP34	DQS0/CSB0#
MD8	AM32	MD8
MD9	AL31	MD9
MD10	AR31	MD10
MD11	AL30	MD11
MD12	AR32	MD12
MD13	AR33	MD13
MD14	AN31	MD14
MD15	AM31	MD15
DQM1	AR32	DQM1
DQS1	AP32	DQS1/CSB1#
MD16	AP30	MD16
MD17	AR30	MD17
MD18	AM29	MD18
MD19	AL27	MD19
MD20	AN30	MD20
MD21	AN29	MD21
MD22	AL28	MD22
MD23	AN28	MD23
DQM2	AL29	DQM2
DQS2	AR29	DQS2/CSB2#
MD24	AP26	MD24
MD25	AN25	MD25
MD26	AR24	MD26
MD27	AL24	MD27
MD28	AL25	MD28
MD29	AR26	MD29
MD30	AM25	MD30
MD31	AN24	MD31
DQM3	AP24	MD31
DQS3	AR25	DQM3/CSB3#
MD32	AN21	MD32
MD33	AP20	MD33
MD34	AN20	MD34
MD35	AL18	MD35
MD36	AM21	MD36
MD37	AR21	MD37
MD38	AL19	MD38
MD39	AM19	MD39
DQM4	AL20	DQM4
DQS4	AR20	DQS4/CSB4#
MD40	AL15	MD40
MD41	AL14	MD41
MD42	AN15	MD42
MD43	AR15	MD43
MD44	AN16	MD44
MD45	AM15	MD45
MD46	AN14	MD46
MD47	AL13	MD47
DQM5	AP16	MD47
DQS5	AR16	DQM5/CSB5#
MD48	AM13	MD48
MD49	AL12	MD49
MD50	AL11	MD50
MD51	AR12	MD51
MD52	AP14	MD52
MD53	AR14	MD53
MD54	AN13	MD54
MD55	AP12	MD55
DQM6	AN12	DQM6
DQS6	AR13	DQS6/CSB6#
MD56	AL10	MD56
MD57	AR11	MD57
MD58	AM9	MD58
MD59	AR9	MD59
MD60	AM11	MD60
MD61	AN11	MD61
MD62	AP10	MD62
MD63	AN9	MD63
DQM7	AN10	DQM7
DQS7	AR10	DQS7/CSB7#

661FX-2

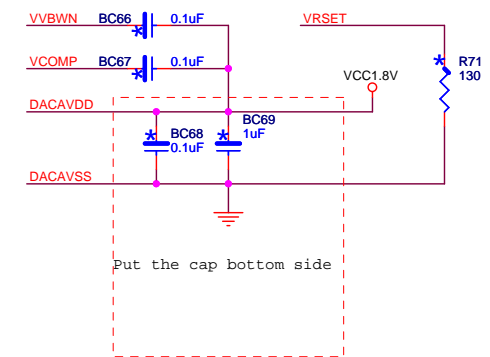
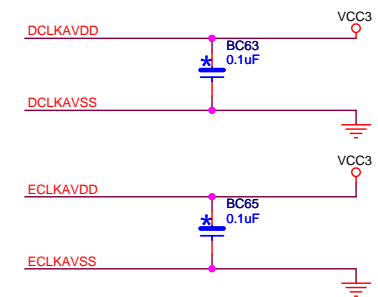
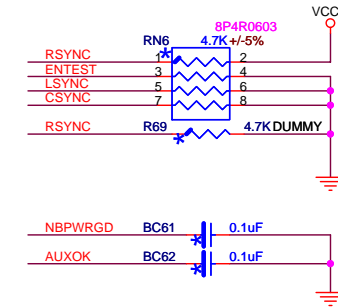
661FX

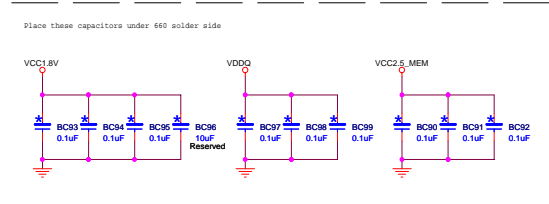
MA0	AR23	MA0
MA1	AN23	MA1
MA2	AN22	MA2
MA3	AM23	MA3
MA4	AL23	MA4
MA5	AL26	MA5
MA6	AN26	MA6
MA7	AN27	MA7
MA8	AR27	MA8
MA9	AR28	MA9
MA10	AP22	MA10
MA11	AN18	MA11
MA12	AR22	MA12
MA13	AP28	MA13
MA14	AM27	MA14
NC	AT1	
SRAS#	AL17	SRAS-
SCAS#	AR19	SCAS-
SWE#	AN19	SWE-
CS0#	AM17	CS-0
CS1#	AL16	CS-1
CS2#	AN17	CS-2
CS3#	AR17	CS-3
CS4#	AP18	
CS5#	AR18	
CKE0	AP4	CKE0
CKE1	AT3	CKE1
CKE2	AR3	CKE2
CKE3	AP3	CKE3
CKE4	AR2	
CKE5	AN4	
S3AUXSW#	AP2	
FBWSDCLKO	AL21	FBWSDCLKO
DRAMTEST	AL22	
LLAVDD	AL35	LLAVDD
LLAVSS	AL34	LLAVSS
DDRAVDD	AM35	DDRAVDD
DDRAVSS	AN36	DDRAVSS
DDRVREFA	AF16	DDRVREFA
DDRVREFB	AF23	DDRVREFB
TRAP2	AP1	
DDRCOMP_P	AR8	DDRCOMP
DDRCOMP_N	AP8	DDRCOMN

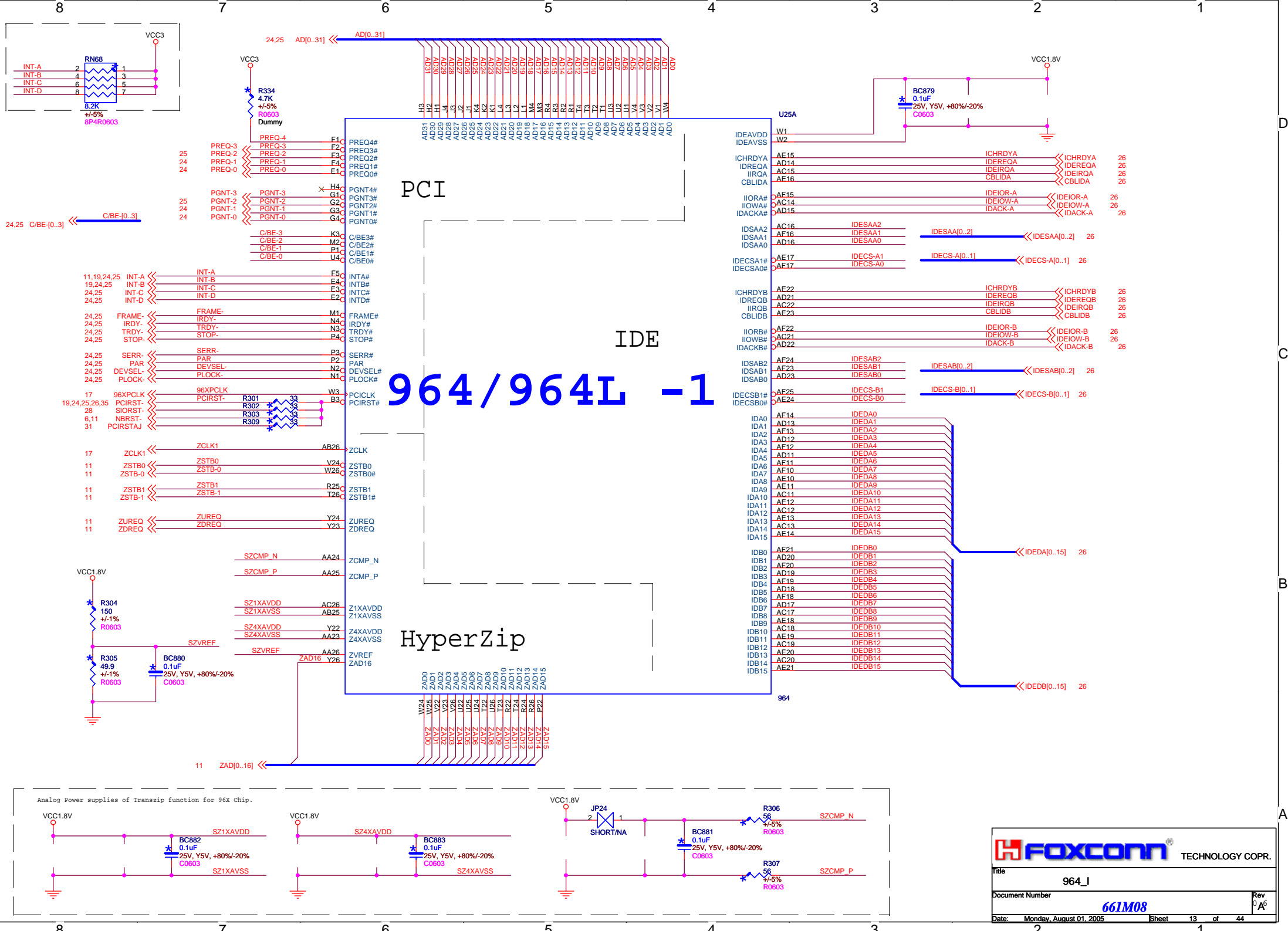


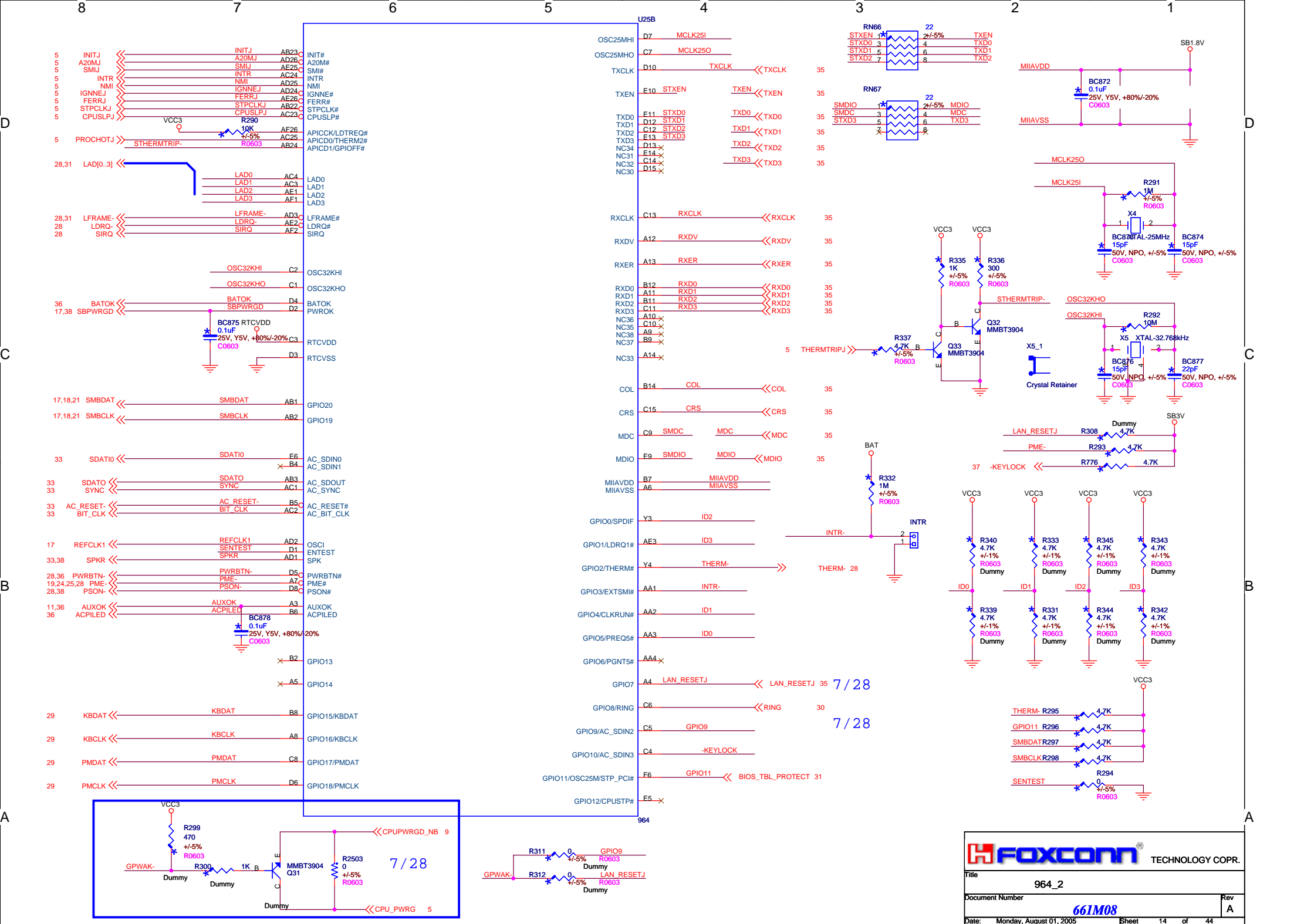


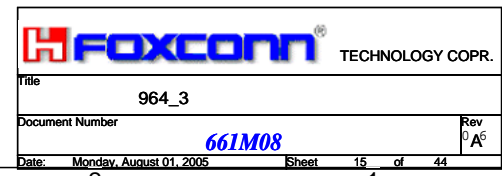
		Enable	Disable
RSYNC	VGA	1	0
LSYNC	panel link	1	0
CSYNC	VB	1	0





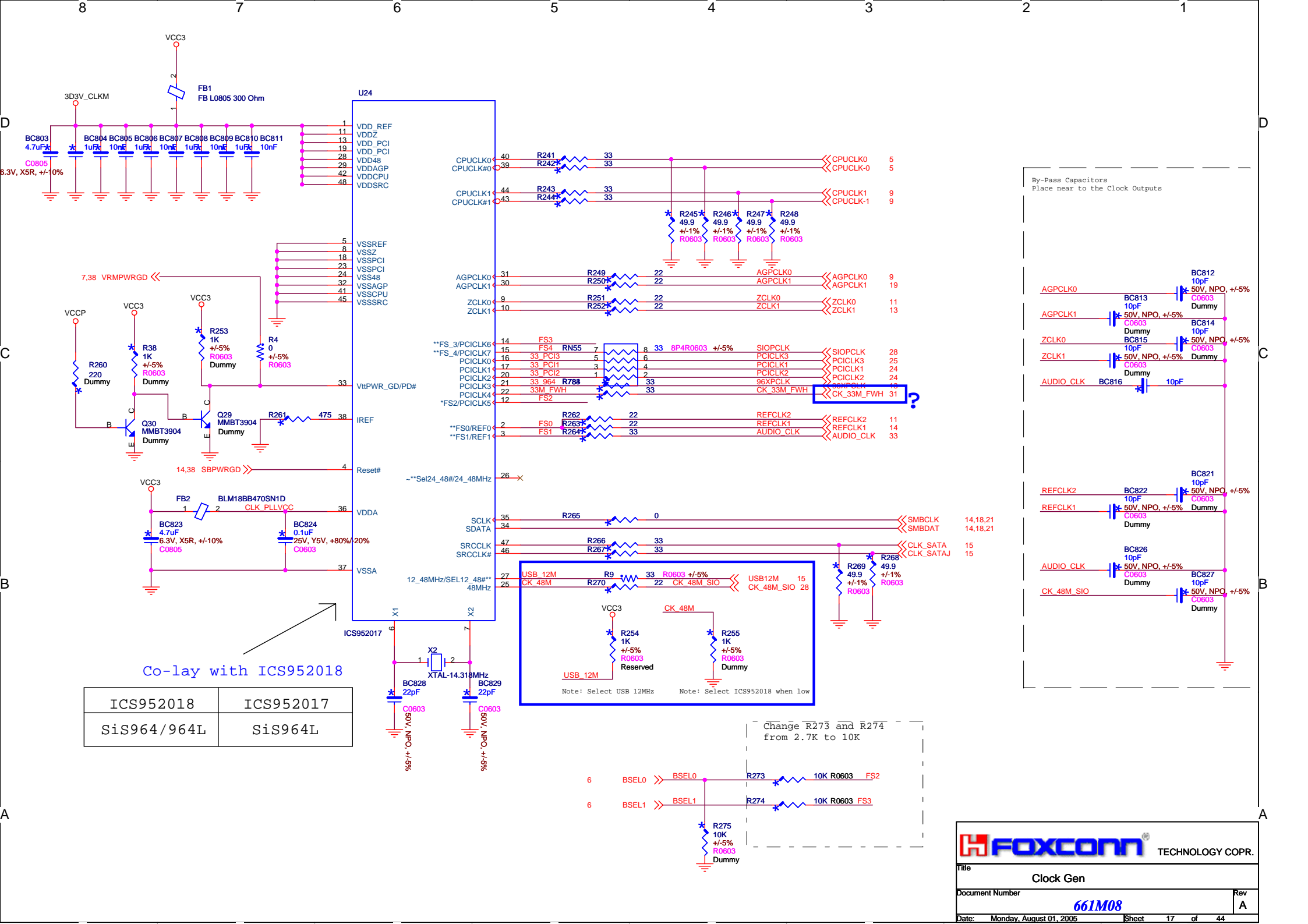


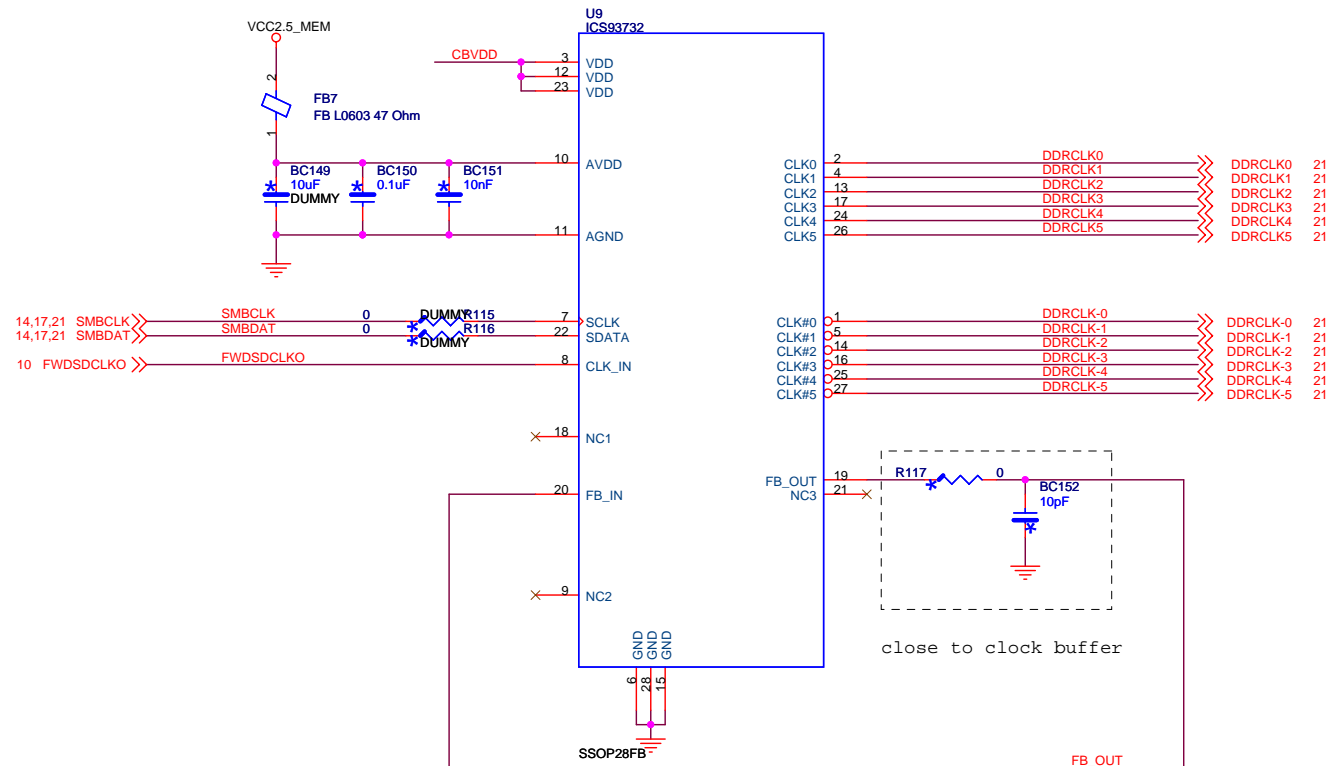
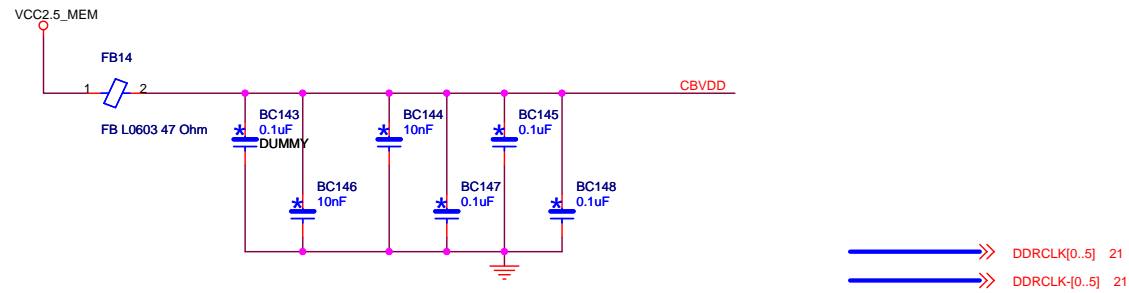






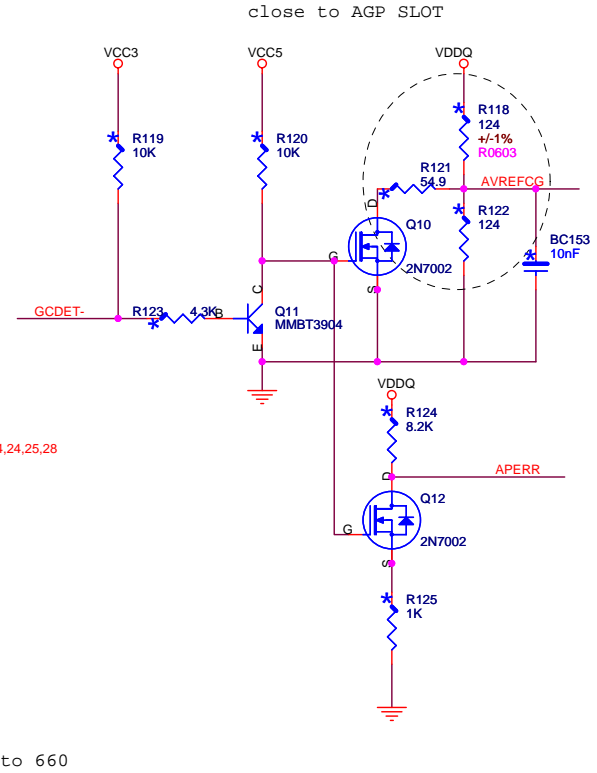
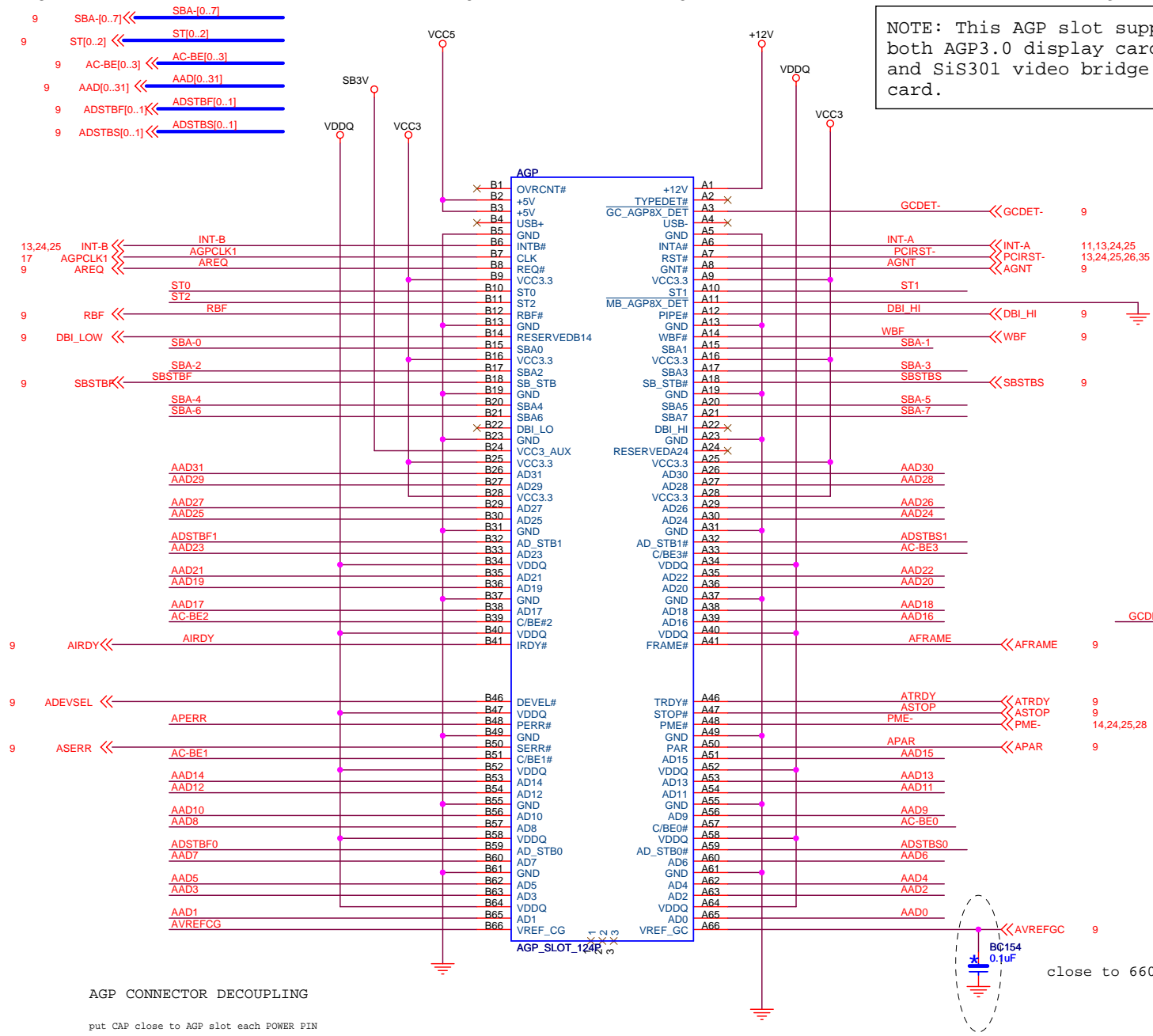






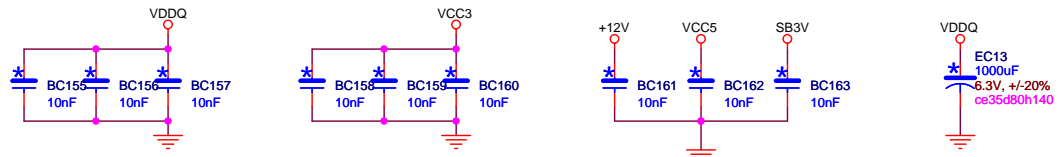
NOTE: This AGP slot support both AGP3.0 display card and SiS301 video bridge card.

GCDET- on card	GCDET-	AVREFCG	APERR
GND	0V	0.35V	0V
OPEN	1.47V	0.75V	1.5V

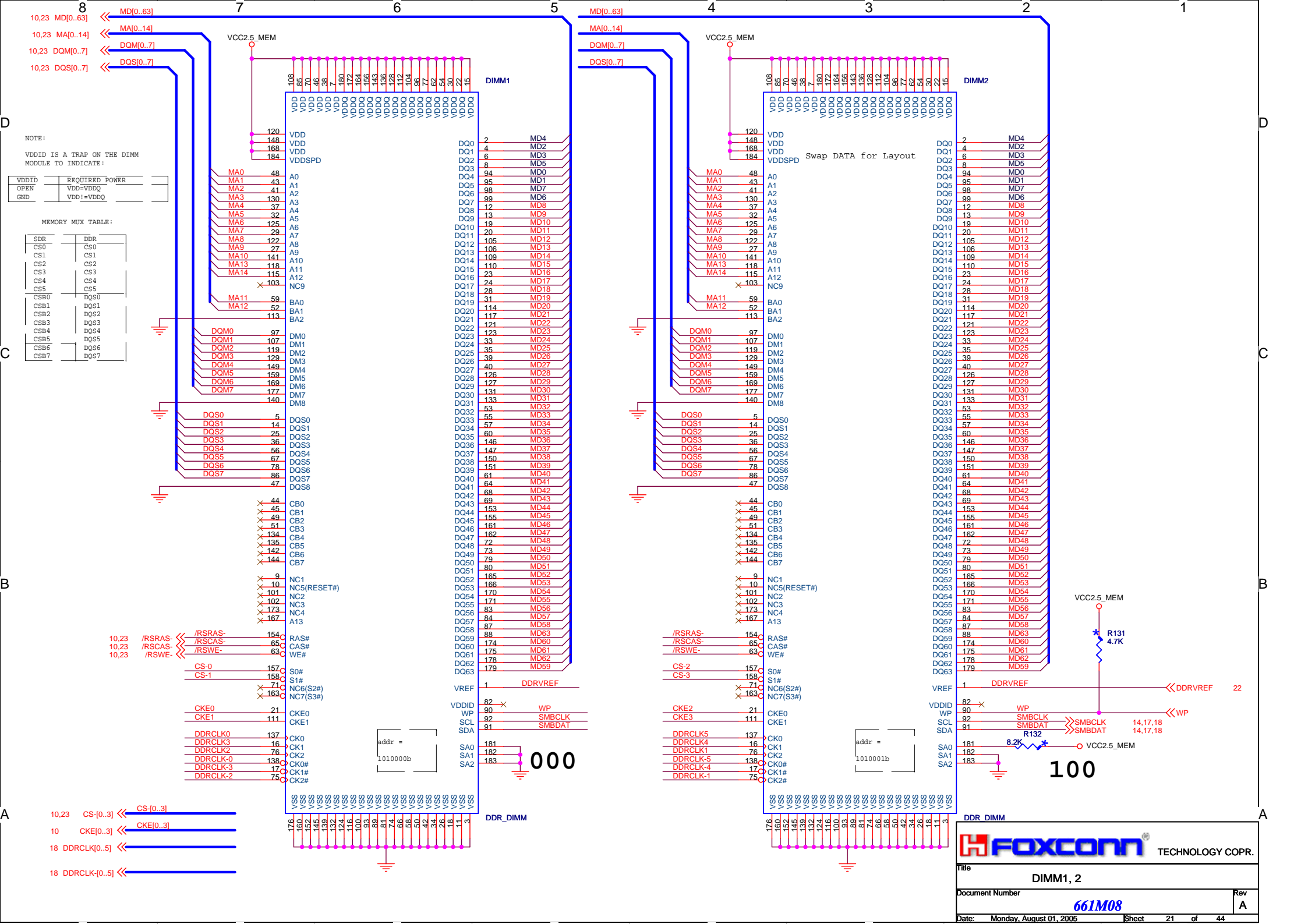


AGP CONNECTOR DECOUPLING

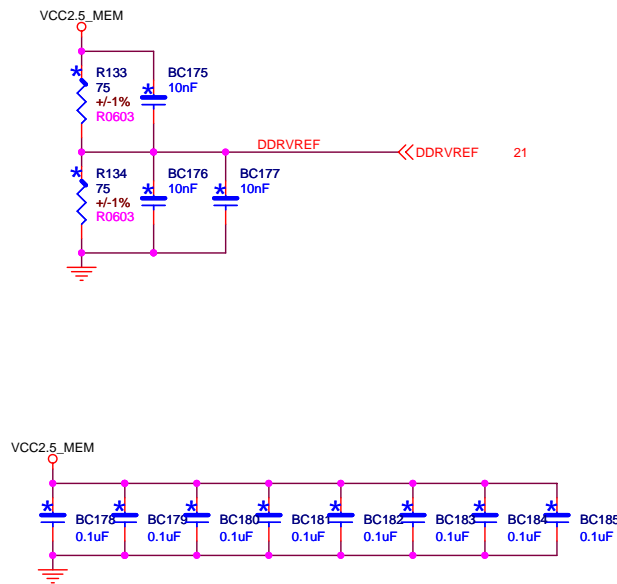
put CAP close to AGP slot each POWER PIN



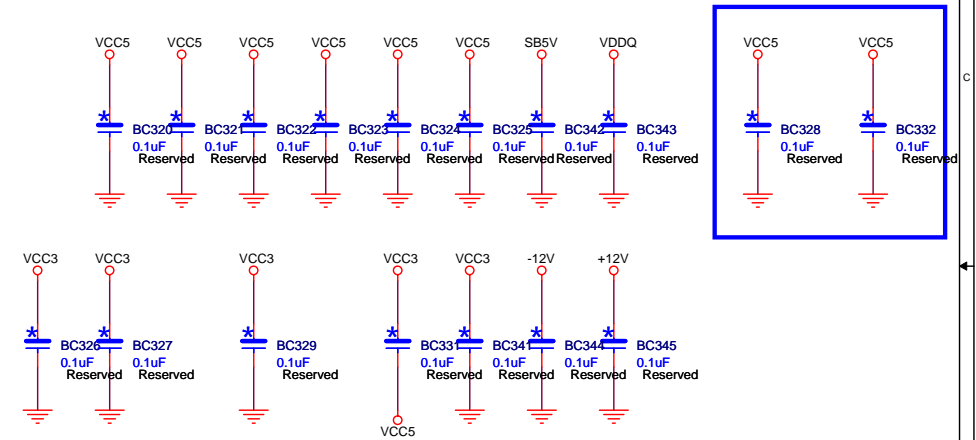




# DDRREF GEN. & DECOUPLING



# EMI

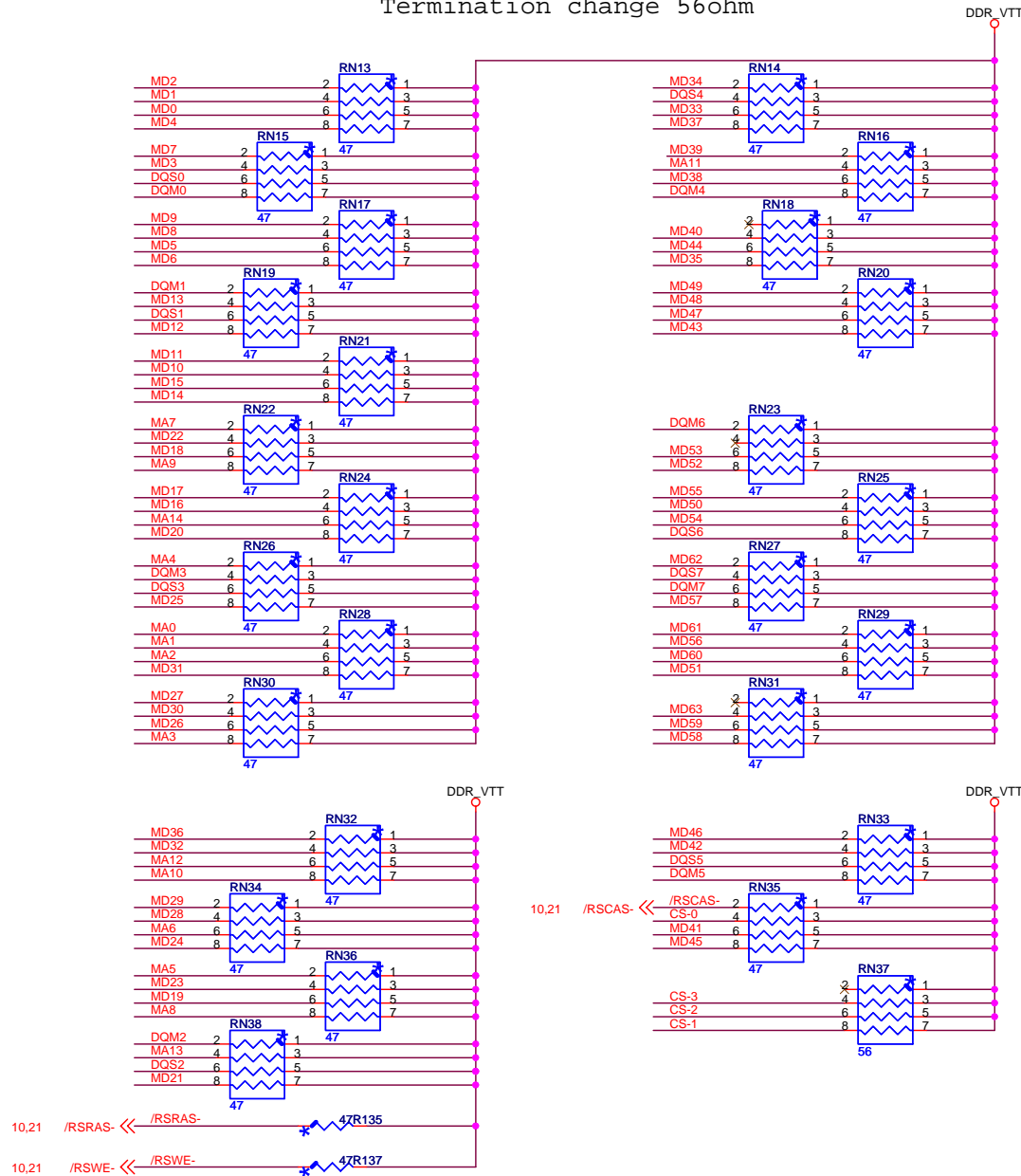


# SSTL-2 Termination Resistors

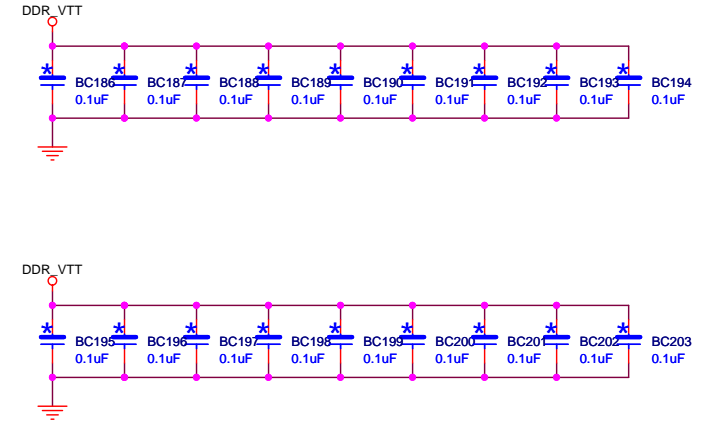
MD[0..63]	<<MD[0..63]	10,21
DQM[0..7]	<<DQM[0..7]	10,21
DQS[0..7]	<<DQS[0..7]	10,21
MA[0..14]	<<MA[0..14]	10,21
CS[0..3]	<<CS[0..3]	10,21

	SDR		DDR		
MD/DQM(/DQS)	LV-CMOS	Rs	SSTL-2	Rs	Rtt
MA/Control	LV-CMOS	0/10/-	SSTL-2	10	33
CS	LV-CMOS	0	SSTL-2	0	33
CKE	DD 3.3V		SSTL-2	0	47
			DD 2.5V		

Termination change 56ohm

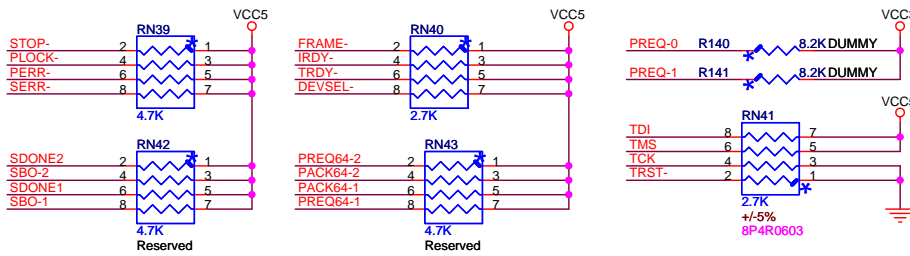
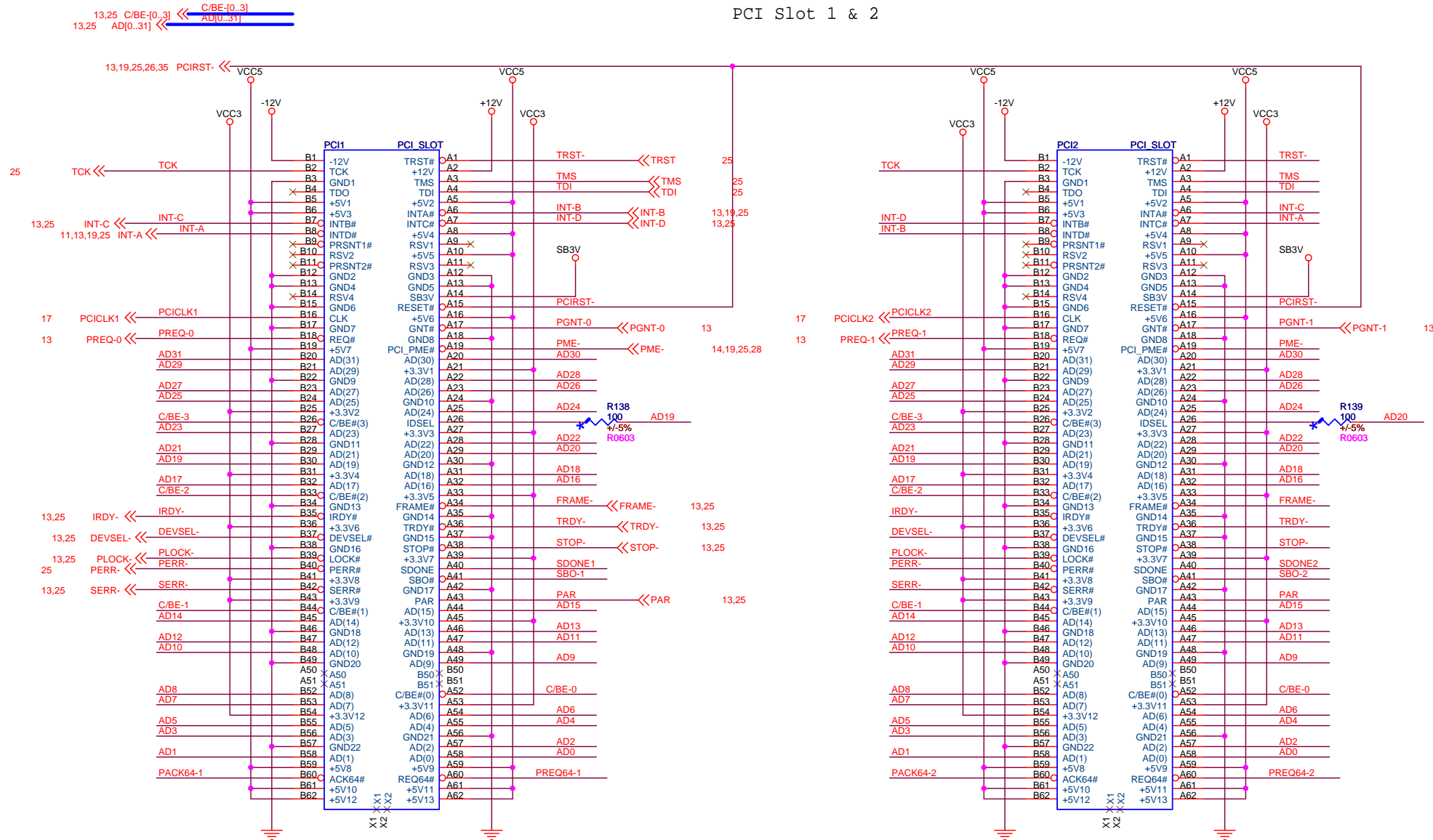


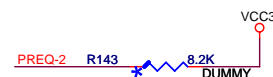
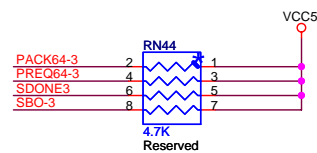
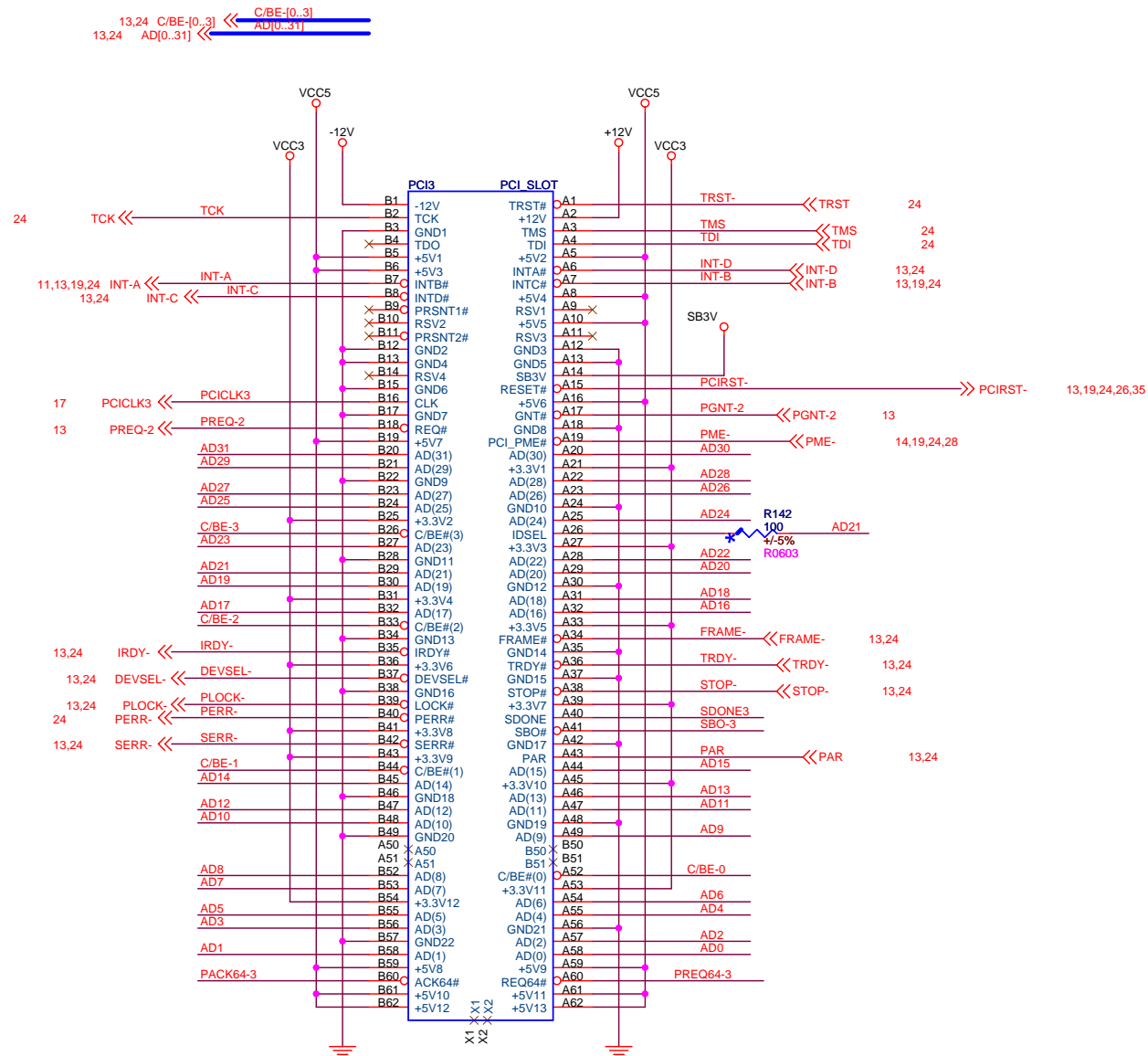
DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND  
0603 Package placed within 200mils of VTT Termination R-packs

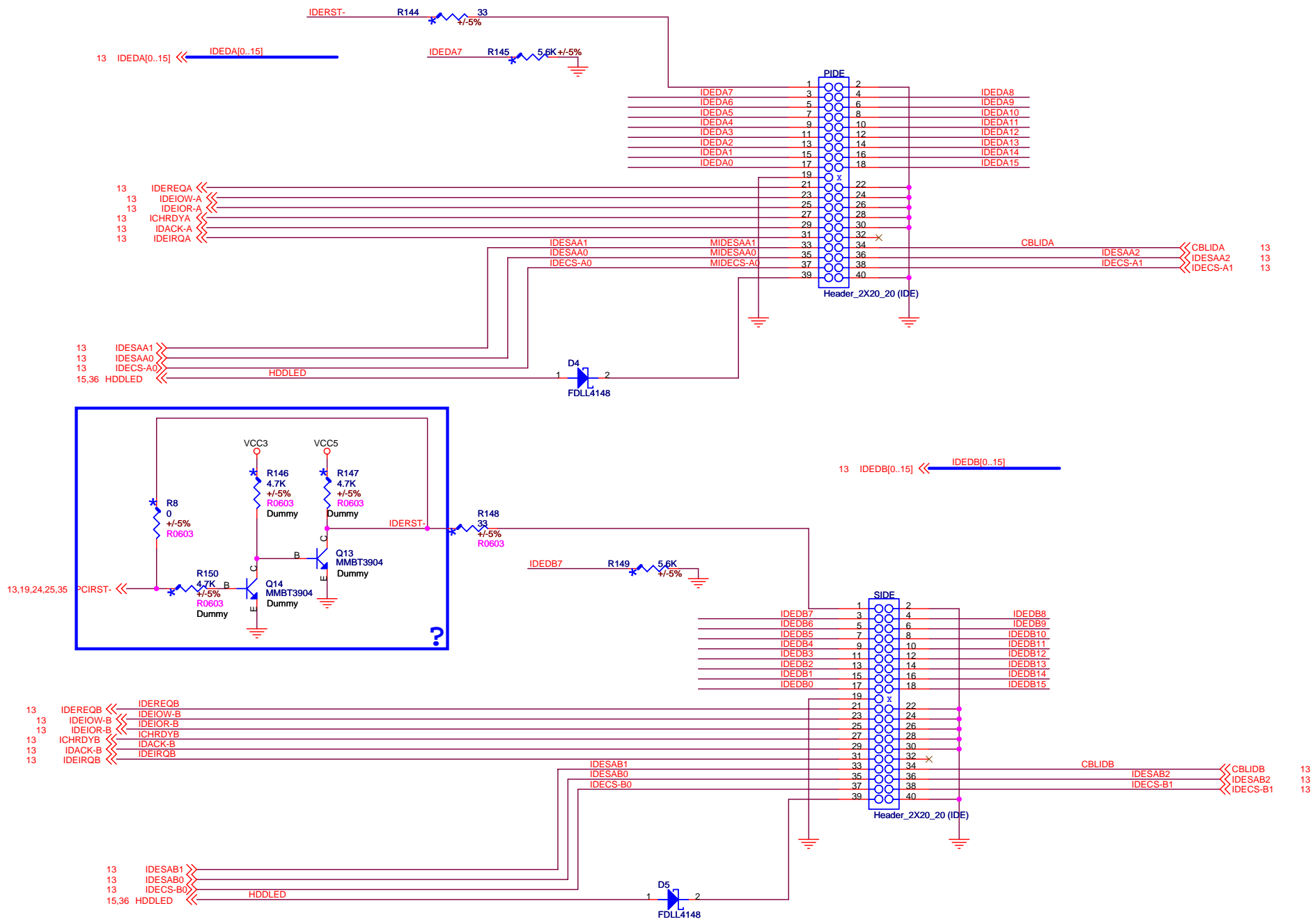


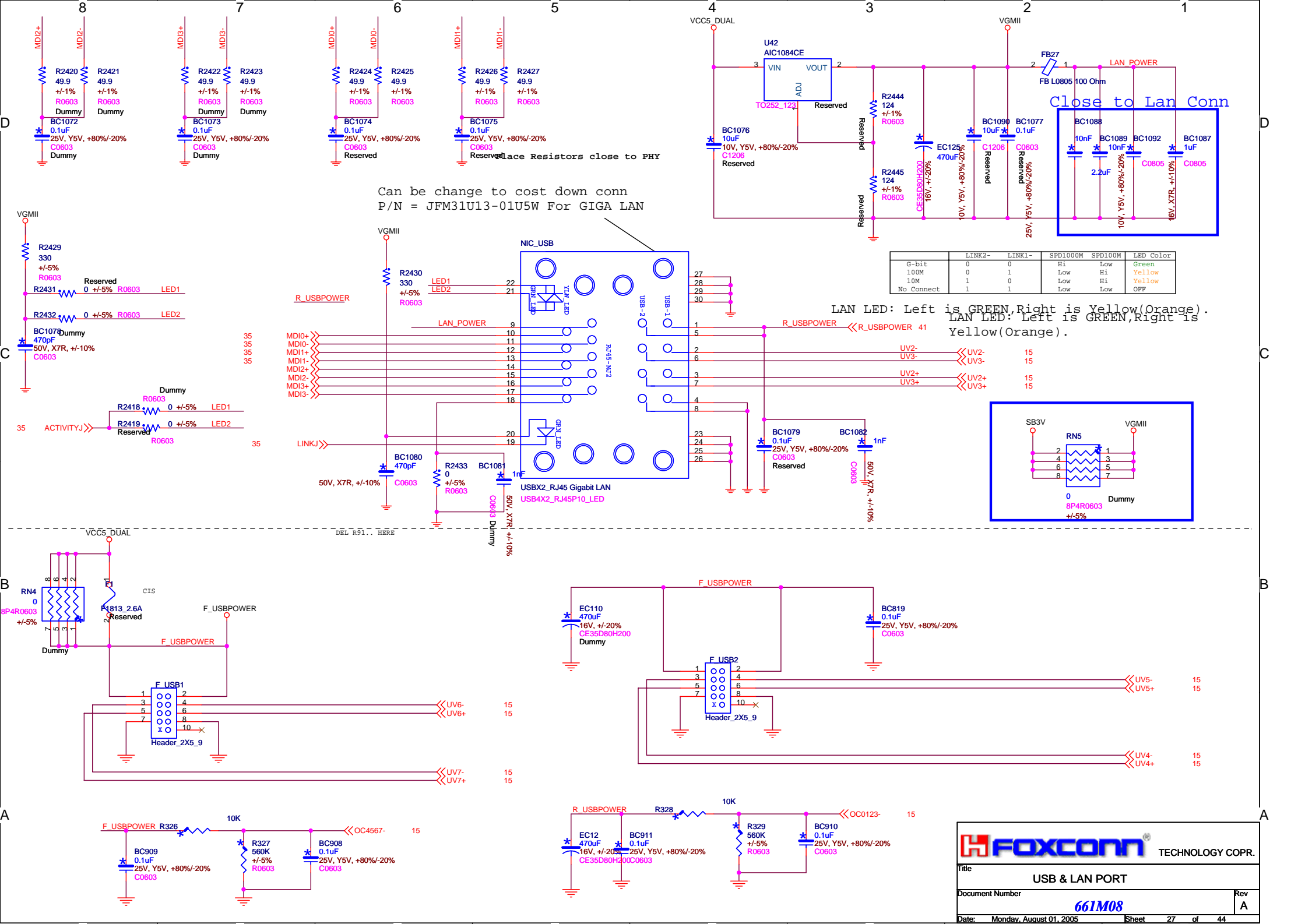


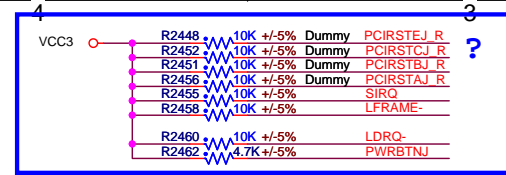
# PCI Slot 1 & 2



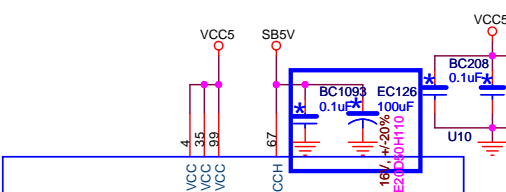
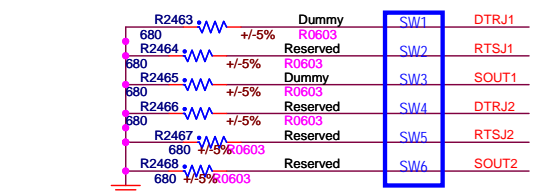




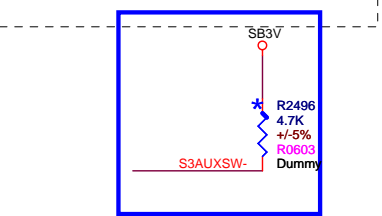
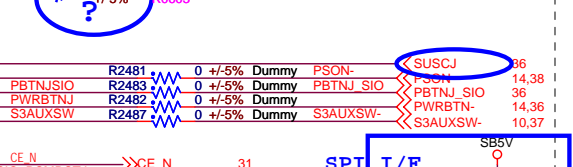
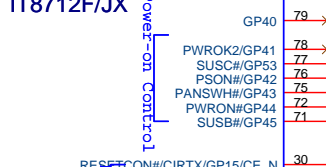
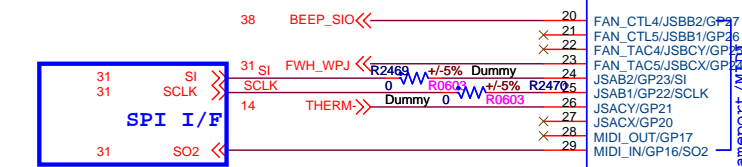
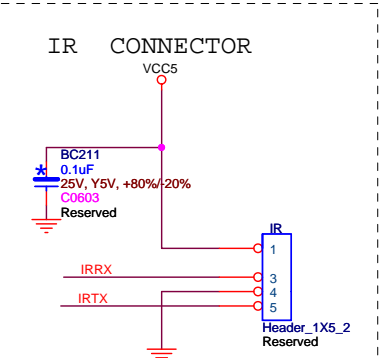
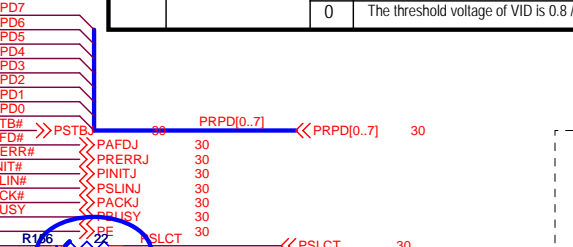
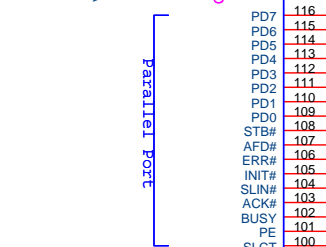
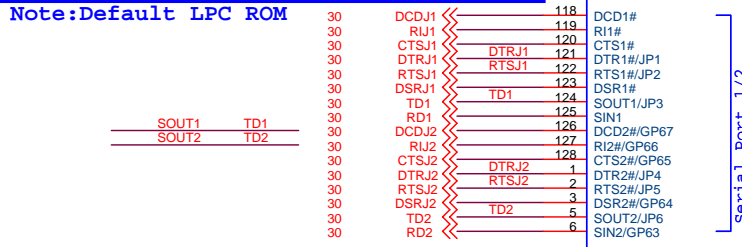




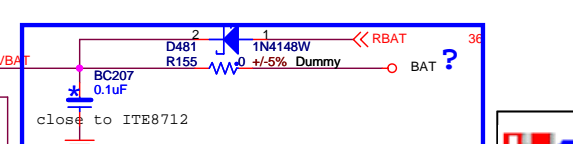
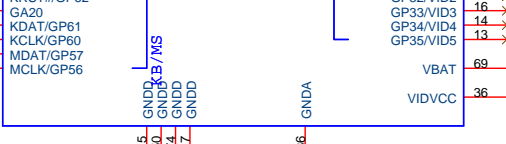
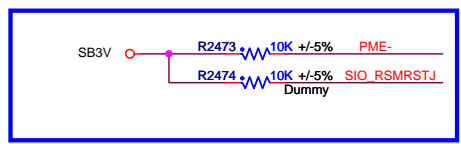
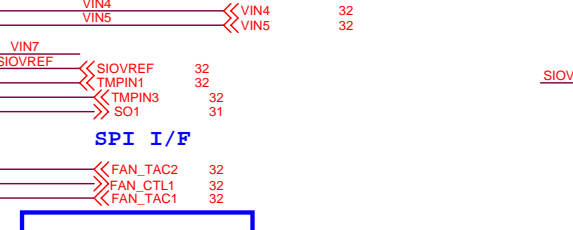
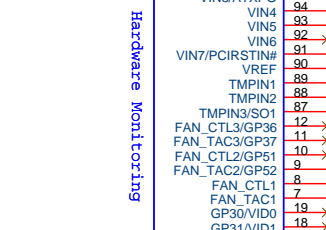
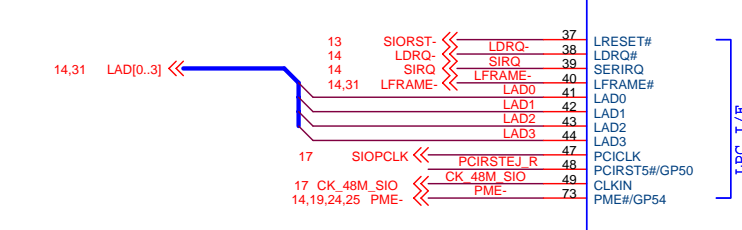
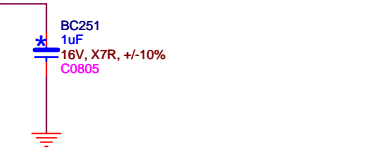
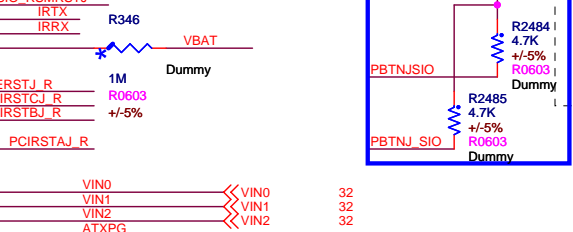
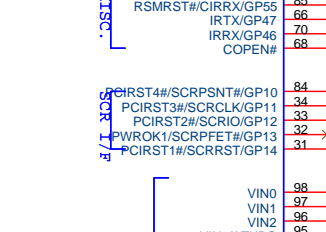
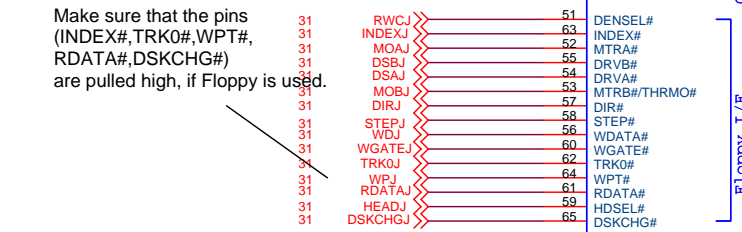
Power On Strapping Options 2			1	
	Symbol	value	Description	Select
SW1	Flashseg1_EN	1	Disabled.	V
		0	Flash I/F Address Segment 1 (FFFF_0000h-FFFF_FFFFh,000F_0000h-000F_FFFFh) is enabled.	
SW2	SerFlh_SO_SEL	1	FLH_S01 is selected as the Serial Flash I/F SO pin.	
		0	FLH_S02 is selected as the Serial Flash I/F SO pin.	V
SW3	CHIP_SEL	--	Chip selection in configuration.	
SW4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10-20 ns when the signal transits from low to high, and then Hi-Z.	
		0	The output buffers are push-pull.	V
SW5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h	
		0	The default value of EC Index 15h / 16h / 17h is 40h	V
SW6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V	
		0	The threshold voltage of VID is 0.8 / 0.4V	V



Note:Default LPC ROM

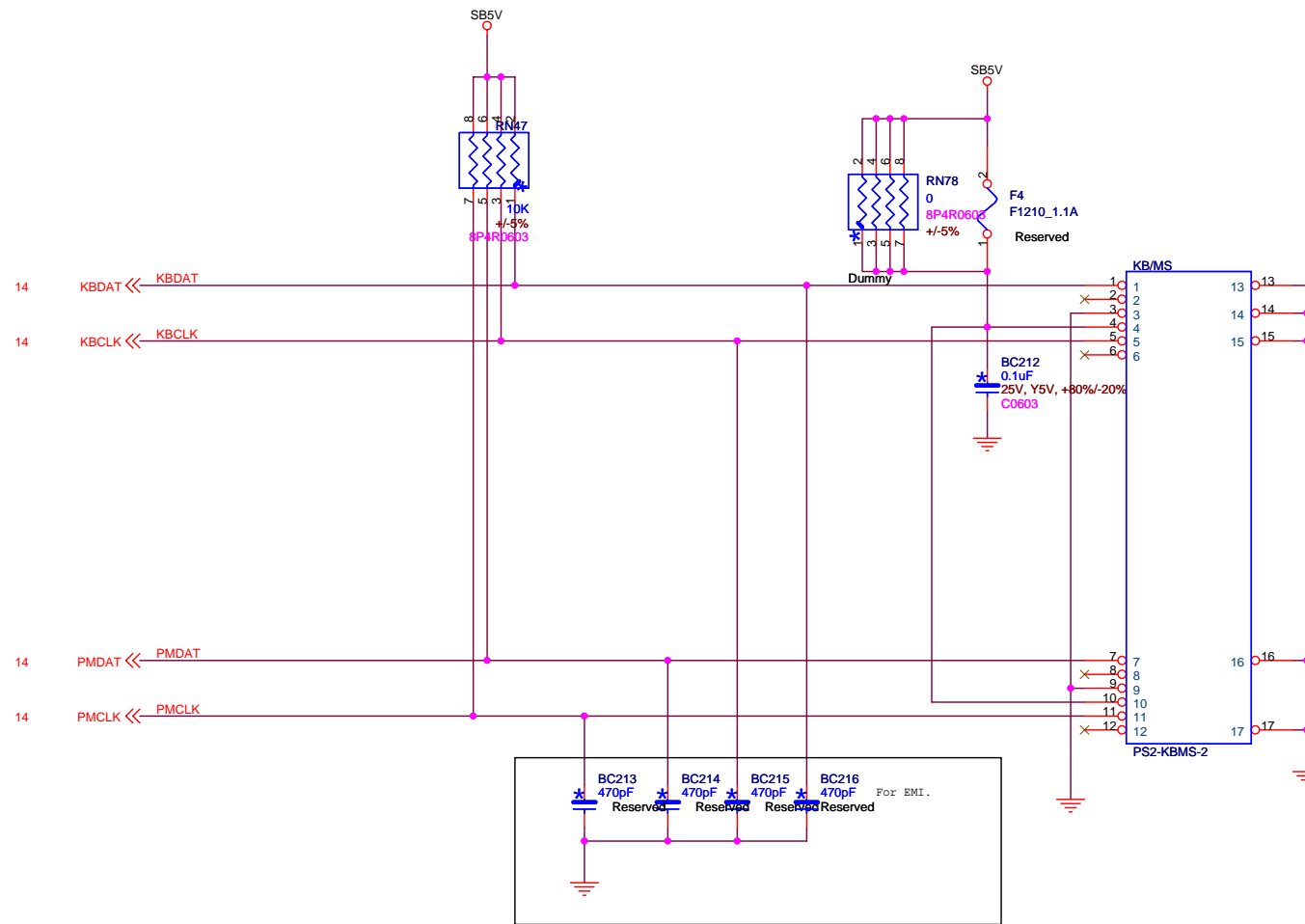


Make sure that the pins  
(INDEX#,TRK0#,WPT#,  
RDATA#,DSKCHG#)  
are pulled high, if Floppy is used.

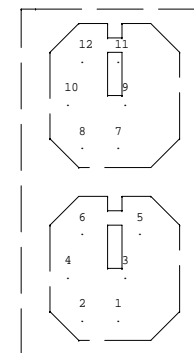


8 7 6 5 4 3 2 1

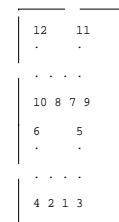
D C B A



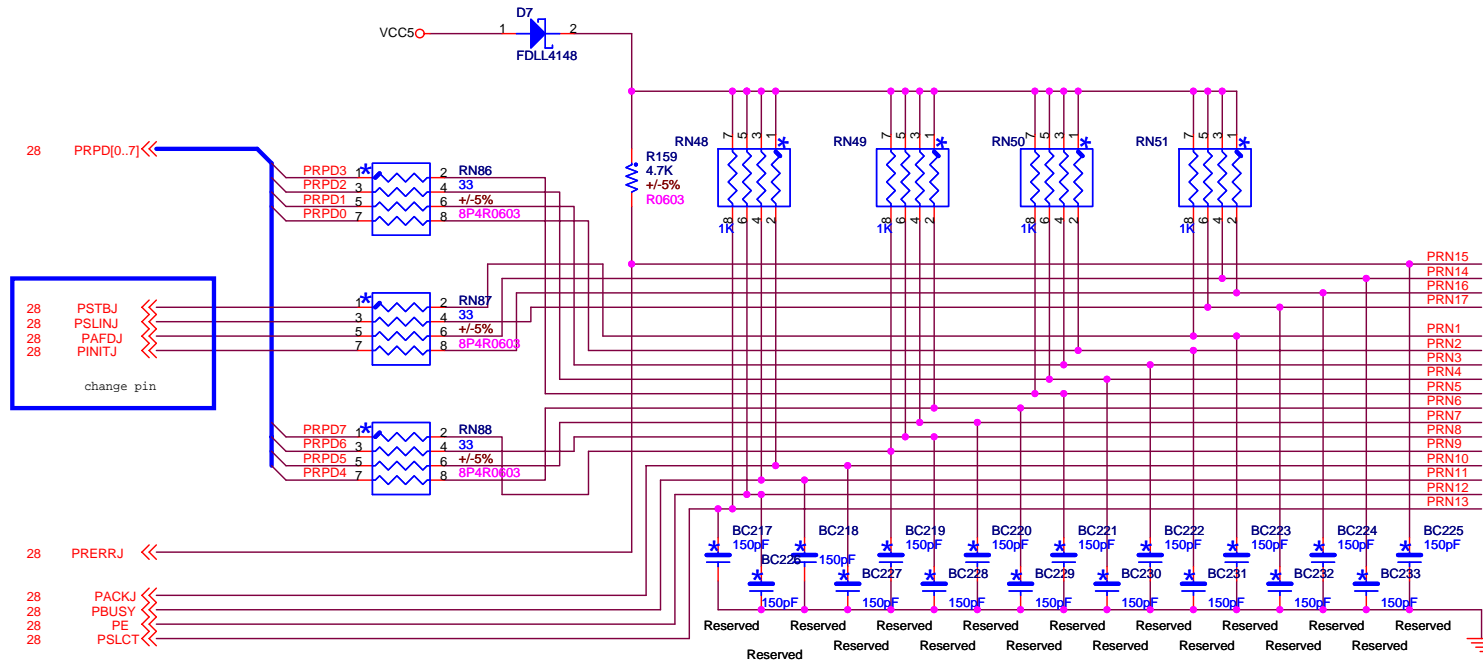
CONNECTOR VIEW



TOP VIEW



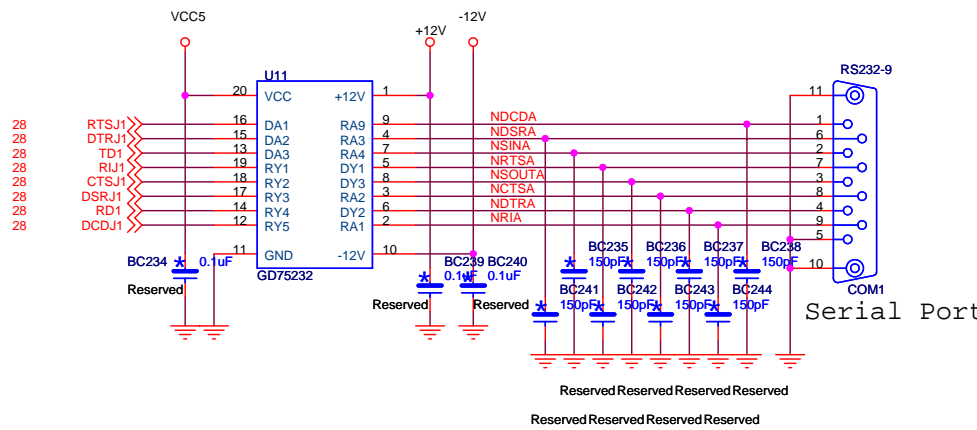
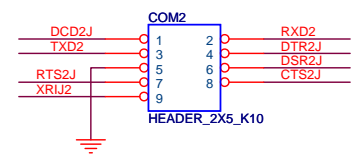
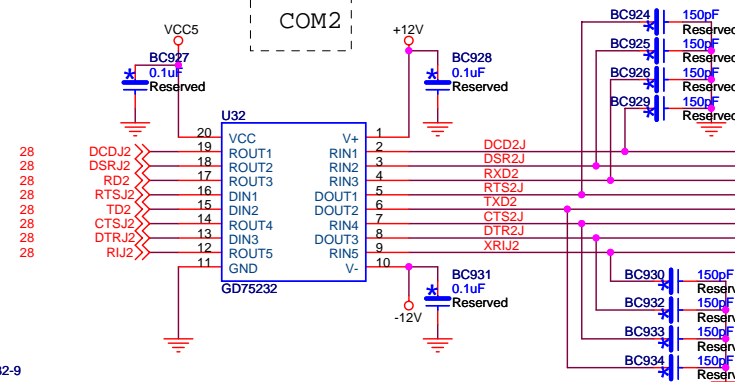
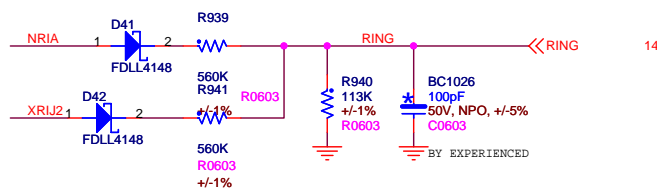
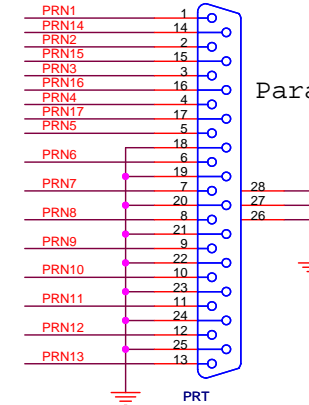
NOTE:  
SIS IS NOT RESPONSIBLE FOR  
ANY ERRORS OR OMISSIONS IN  
THESE SCHEMATICS. THIS IS  
AN EXAMPLE ONLY.



PRINT PORT

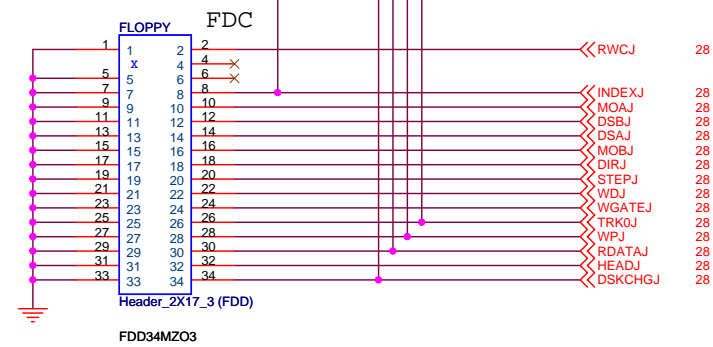
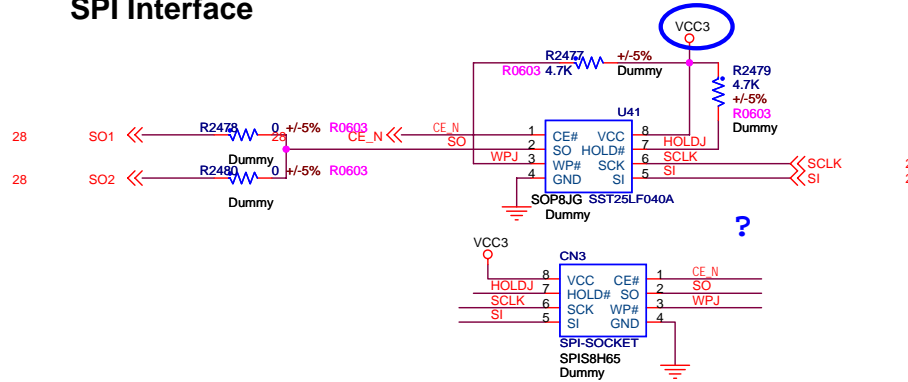
PRNT25-M

Parallel Port

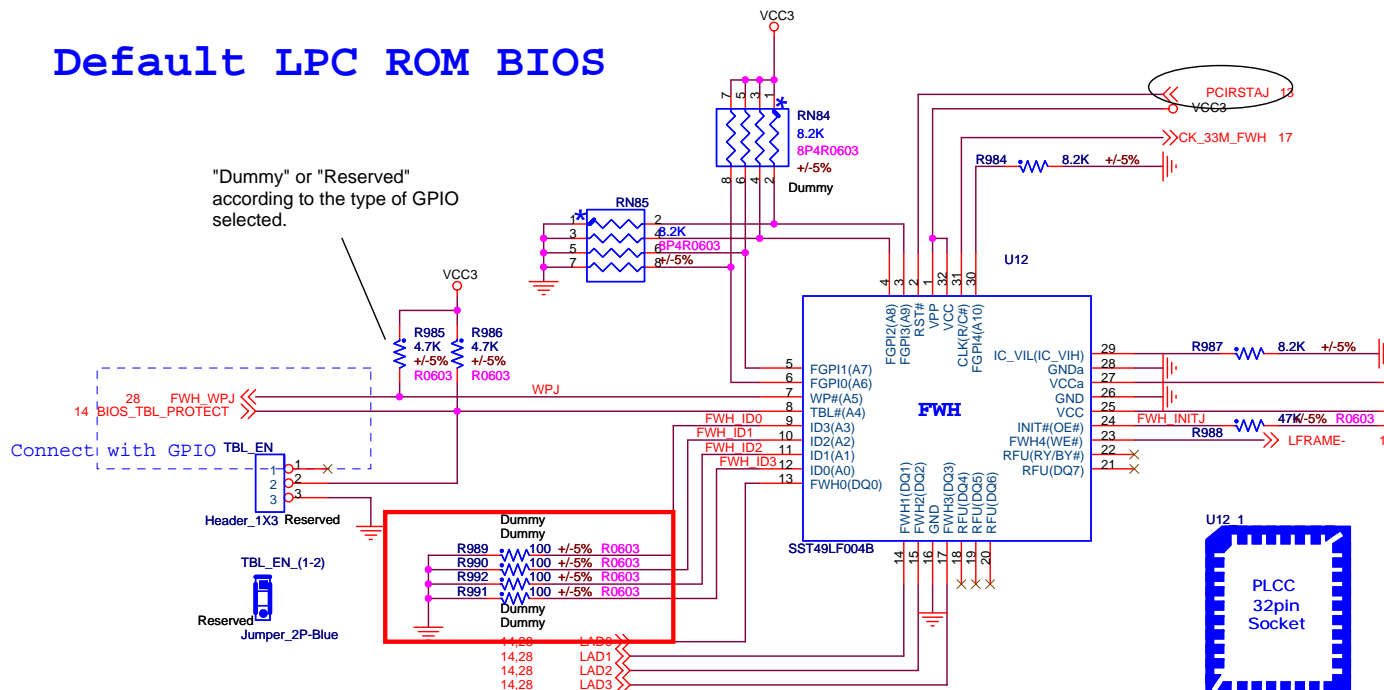


Serial Port

## SPI Interface

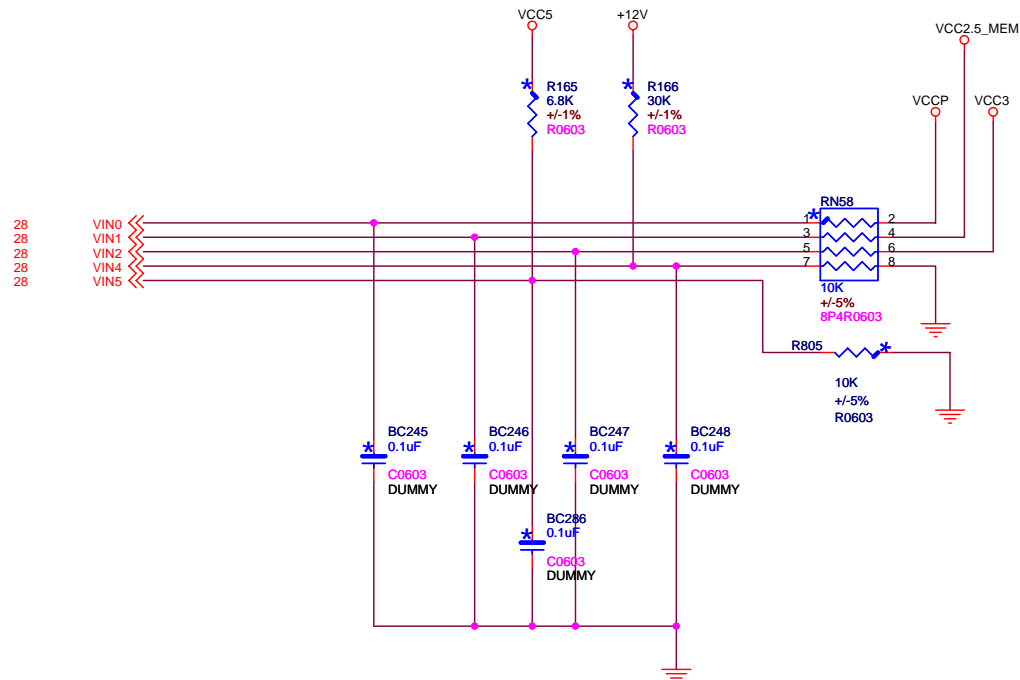


## Default LPC ROM BIOS



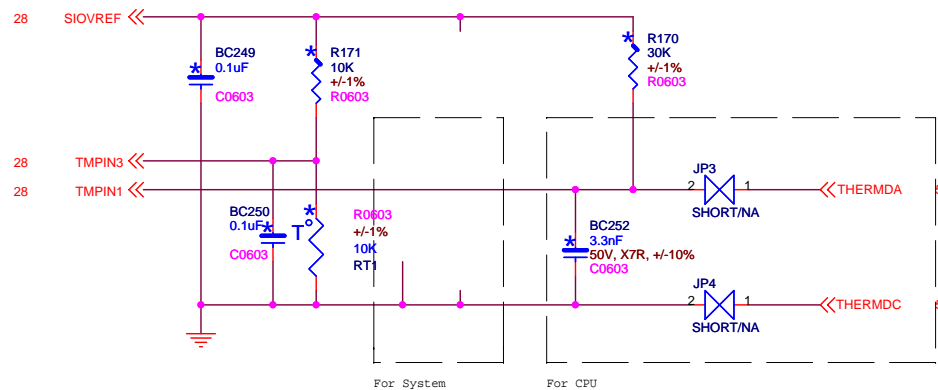


## Voltage Monitor

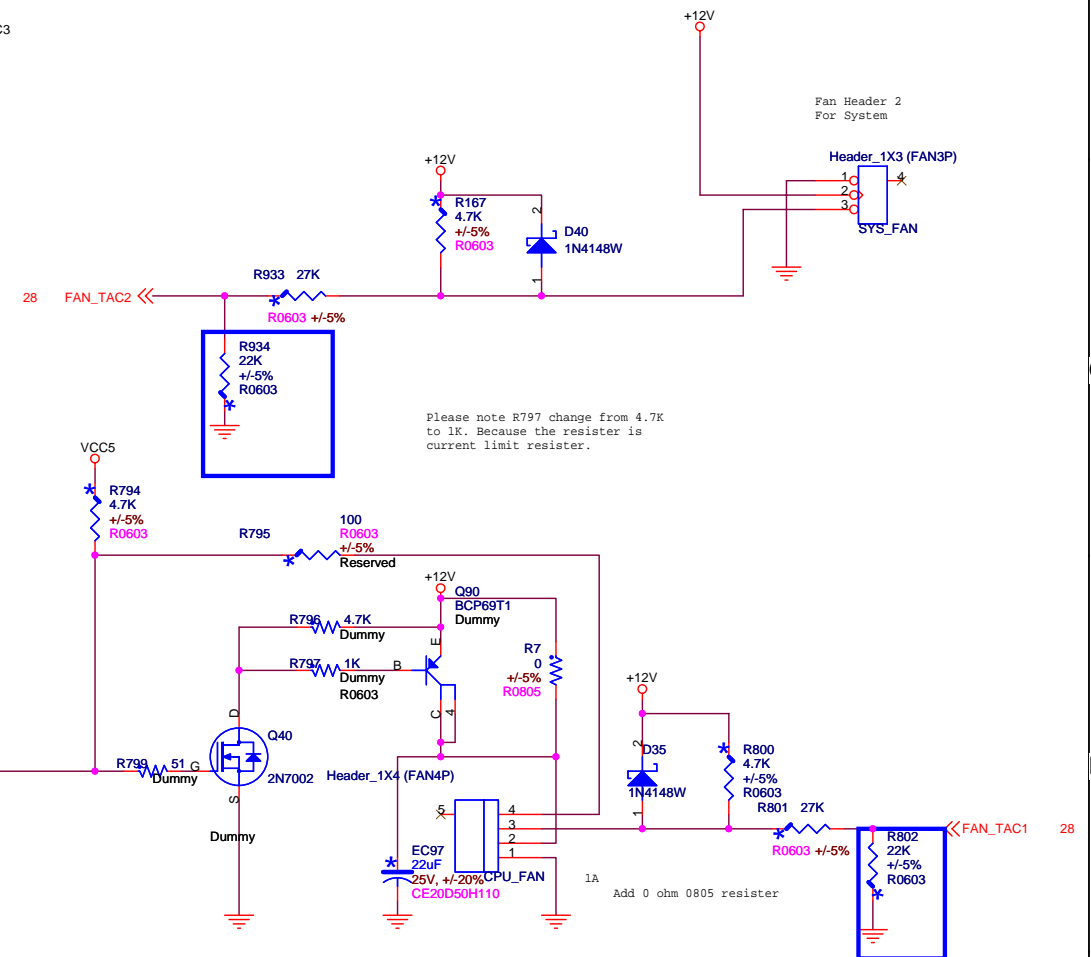


# Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode

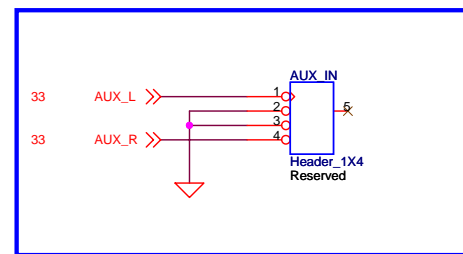
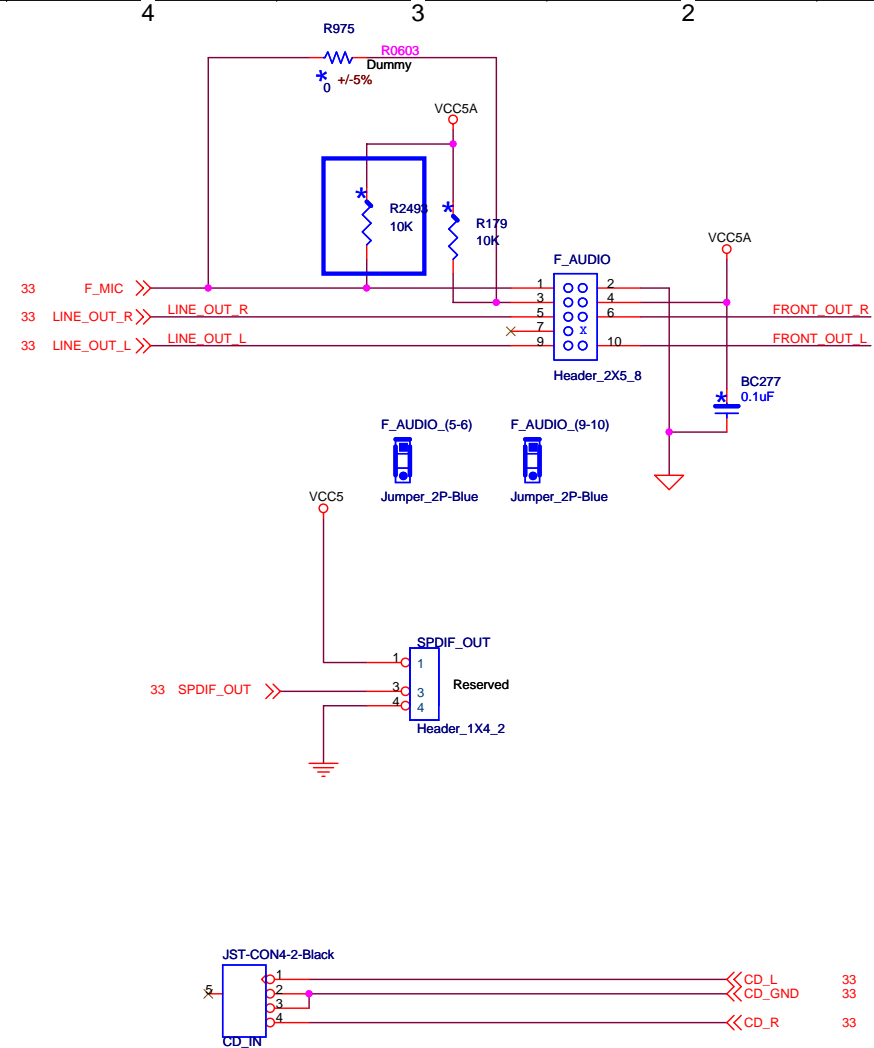
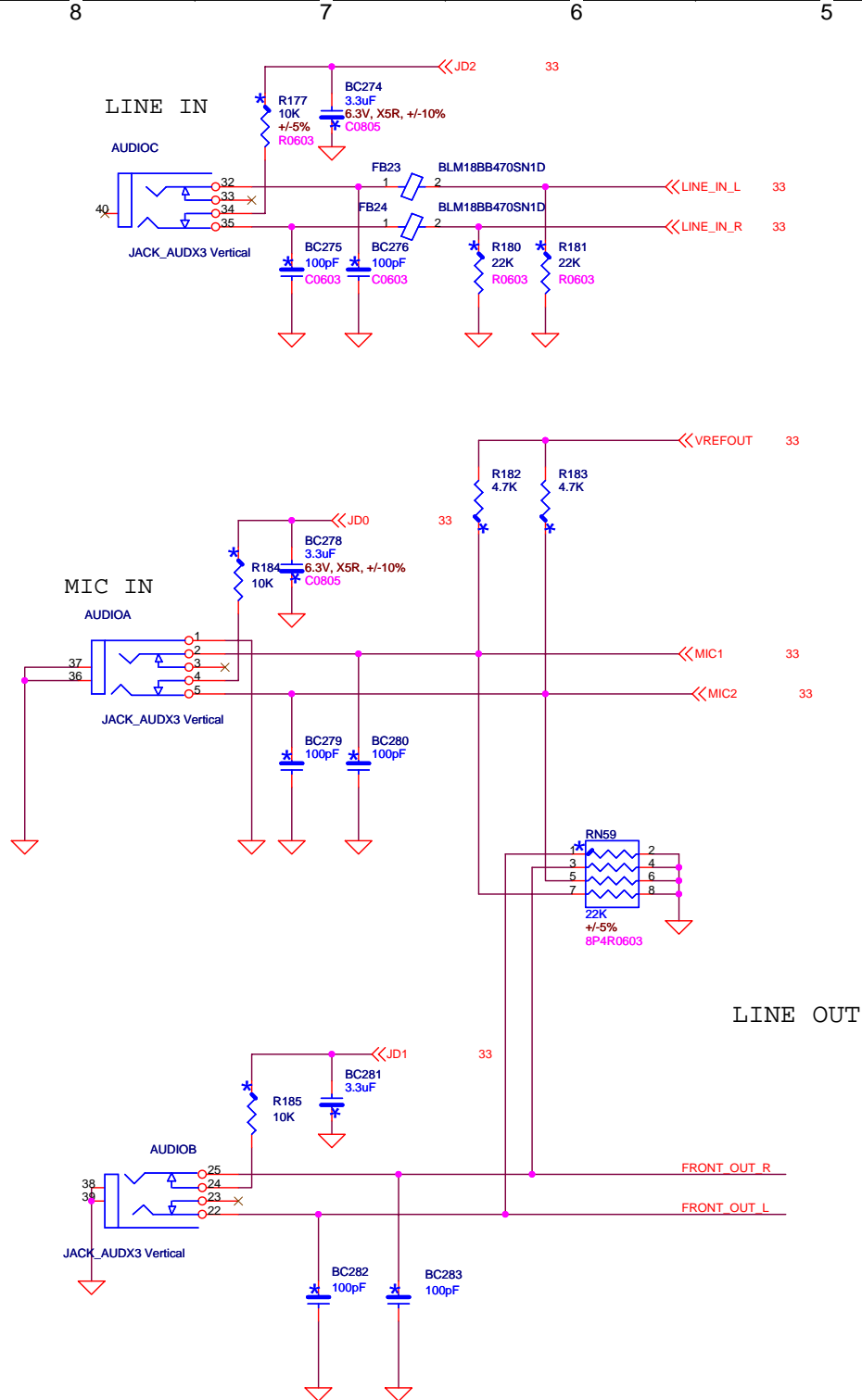


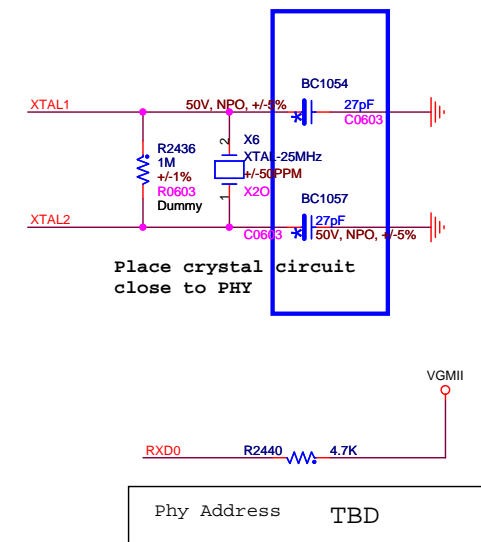
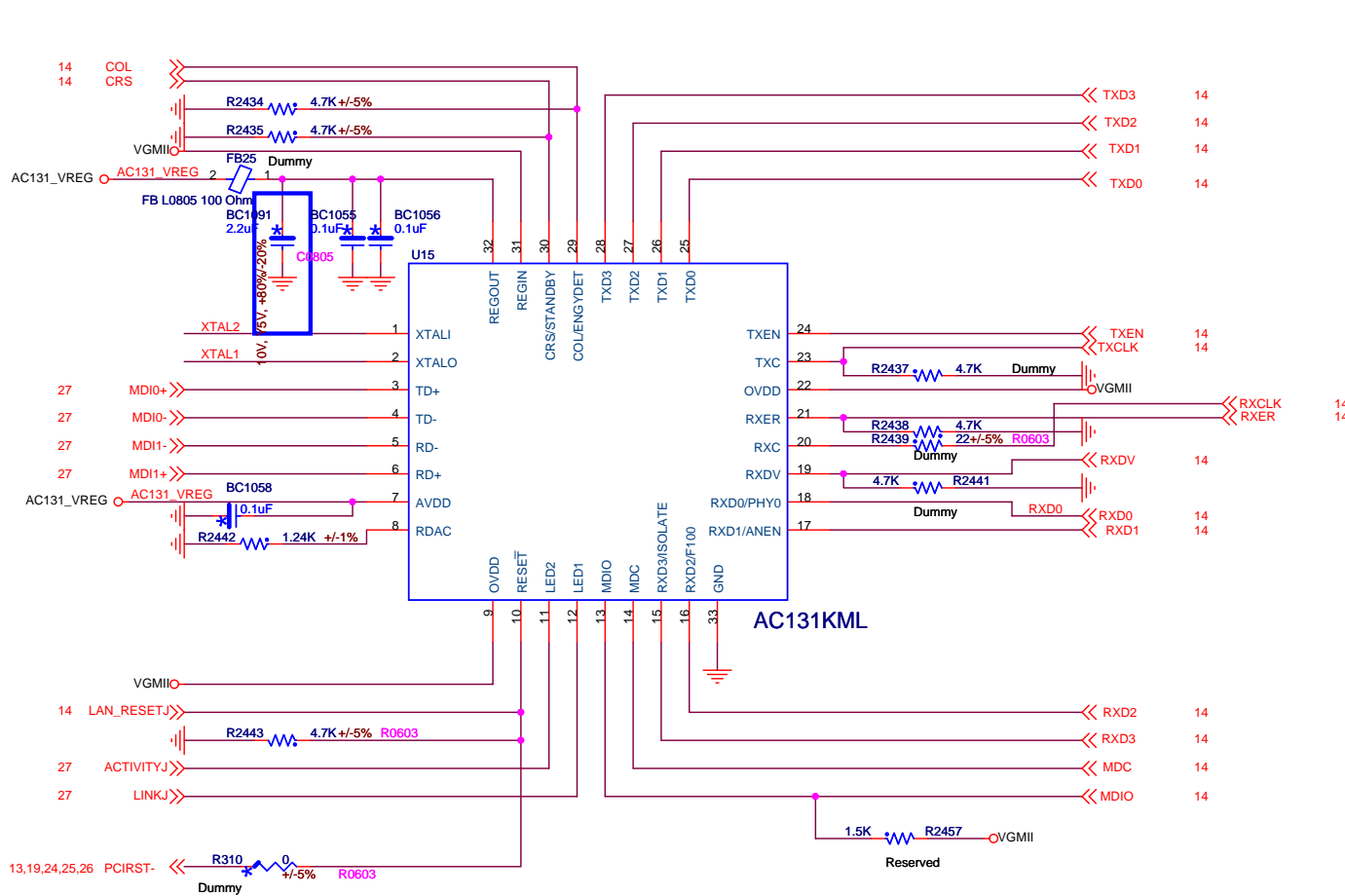
## FAN Input and Output

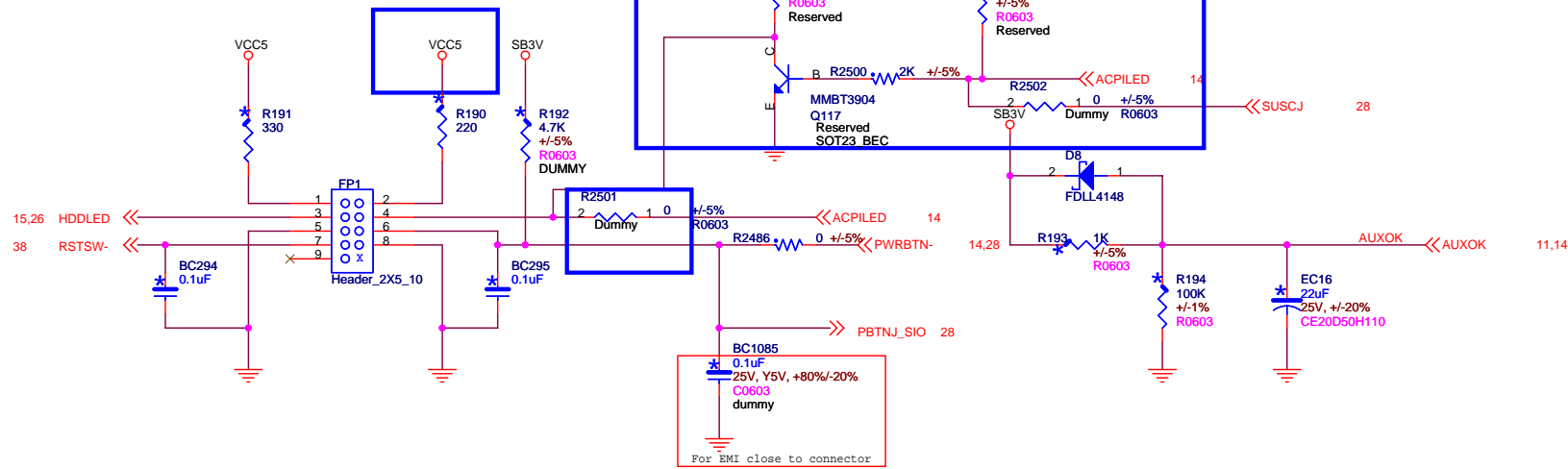


```
check CPU FAN
```





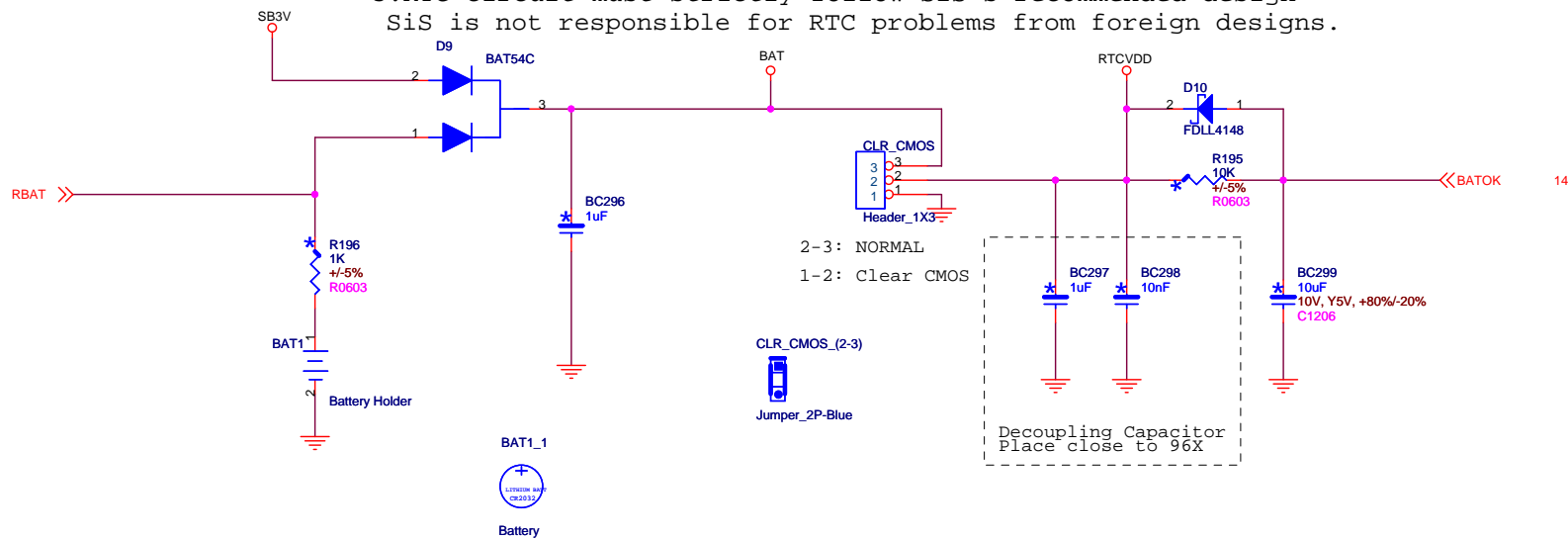




# RTC

## NOTE!

- 1.The RTCVDD is 3V
  - 2.Decoupling capacitor must be close to 96X RTCVDD pin.
  - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.



**5V DUAL CIRCUIT**

**DDR 2.5V CIRCUIT**

**FOXCONN TECHNOLOGY CORP.**

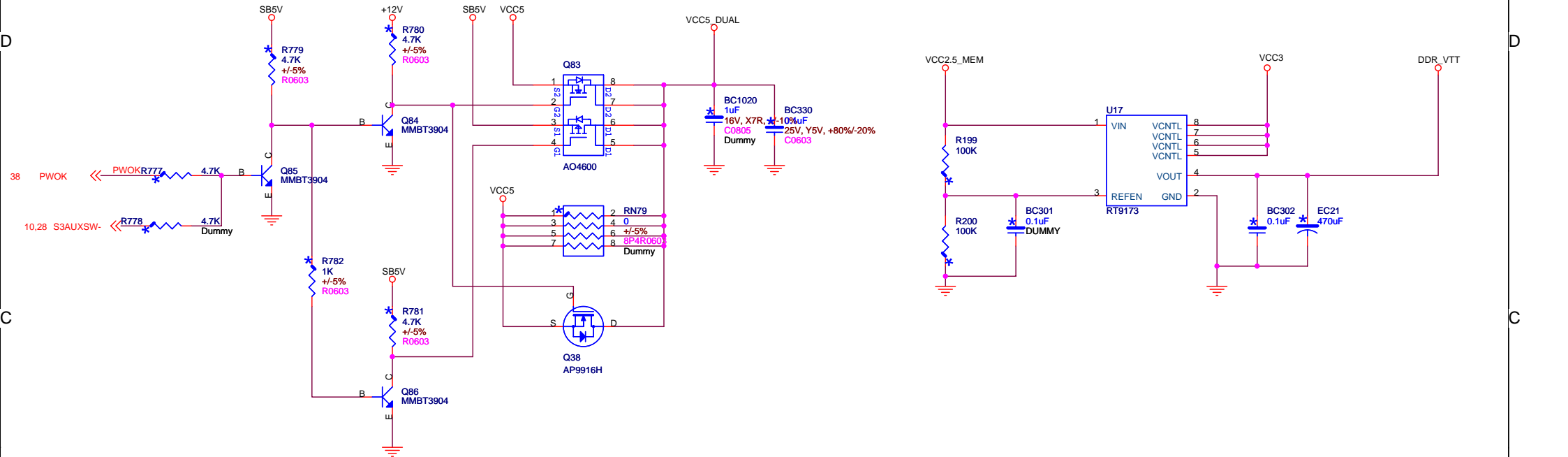
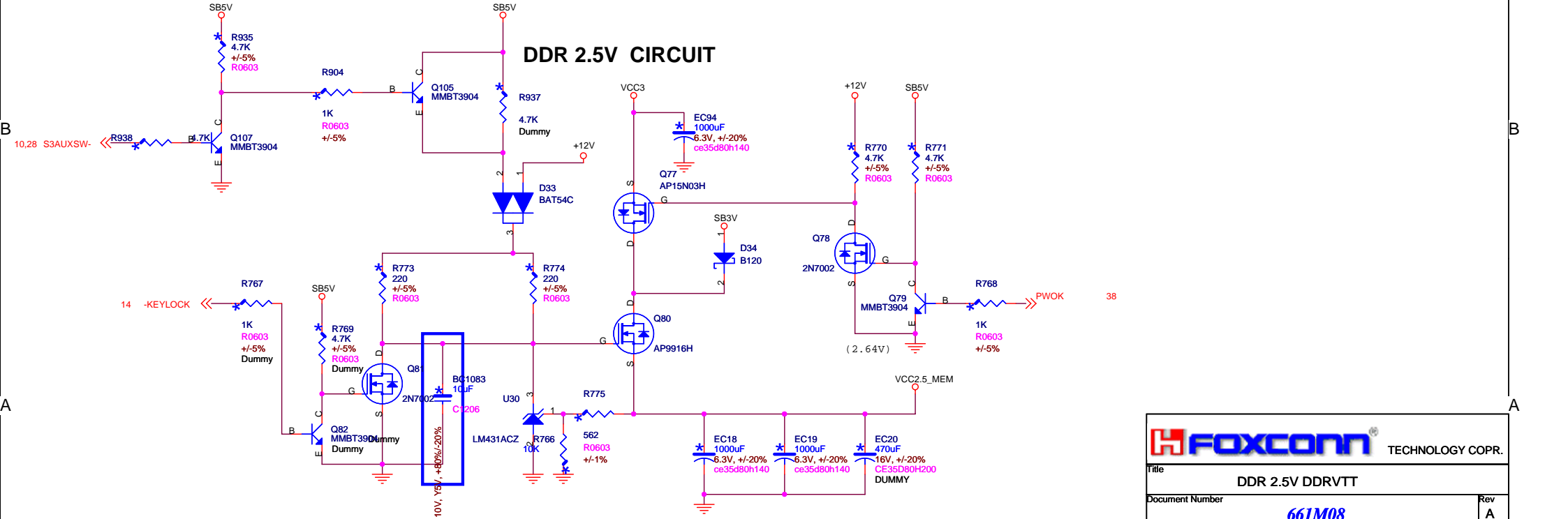
**DDR 2.5V DDRVTT**

**661M08**

**Rev A**

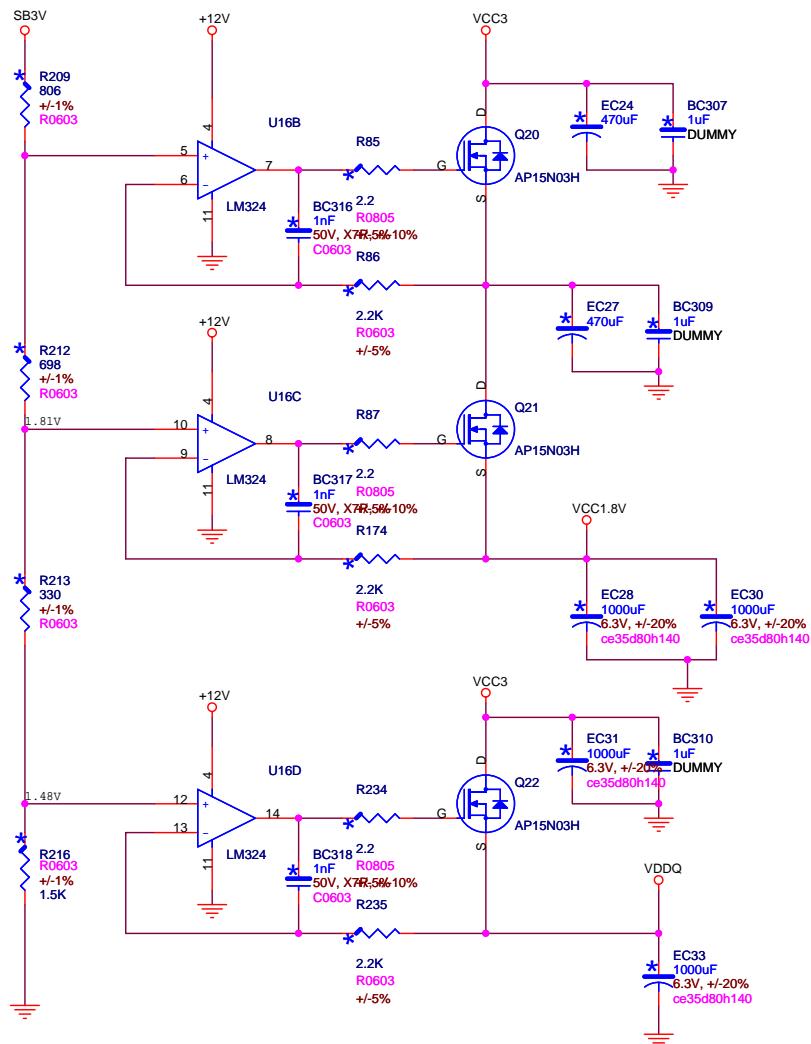
**Date: Monday, August 01, 2005**

**Sheet 37 of 42**

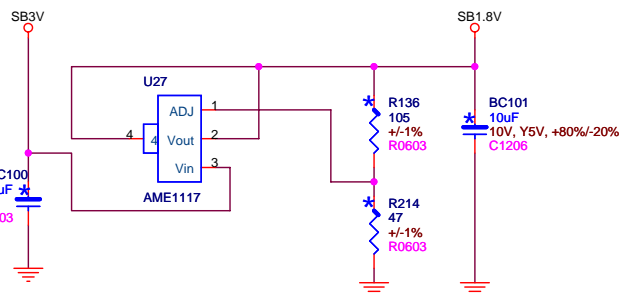
[illegible]



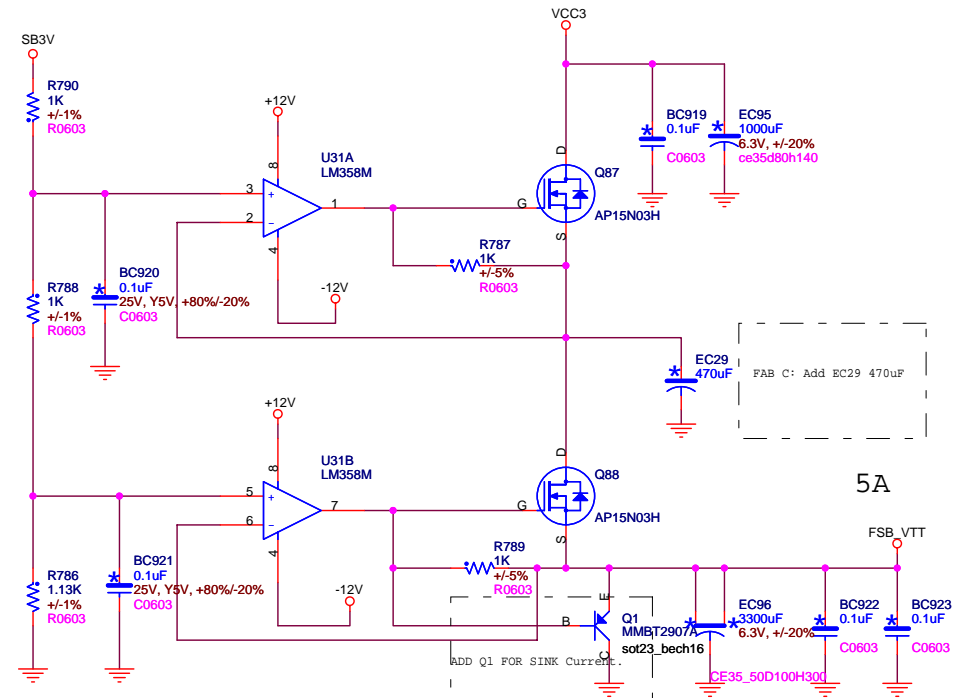
## VCC1.8V and VDDQ



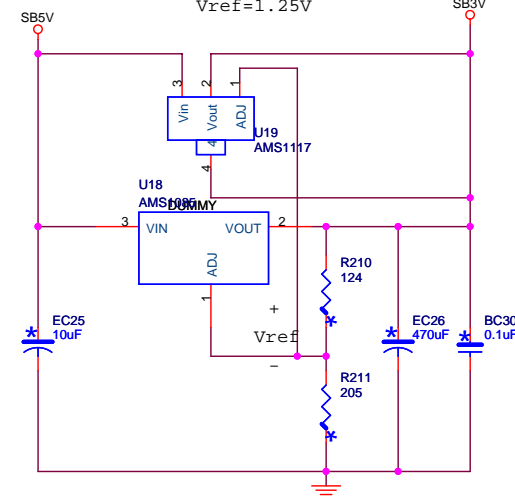
## SB1.8V for 964



## FSB\_VTT

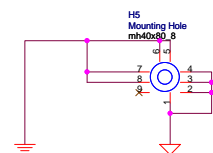



## SB3.3V Vref=1.25V

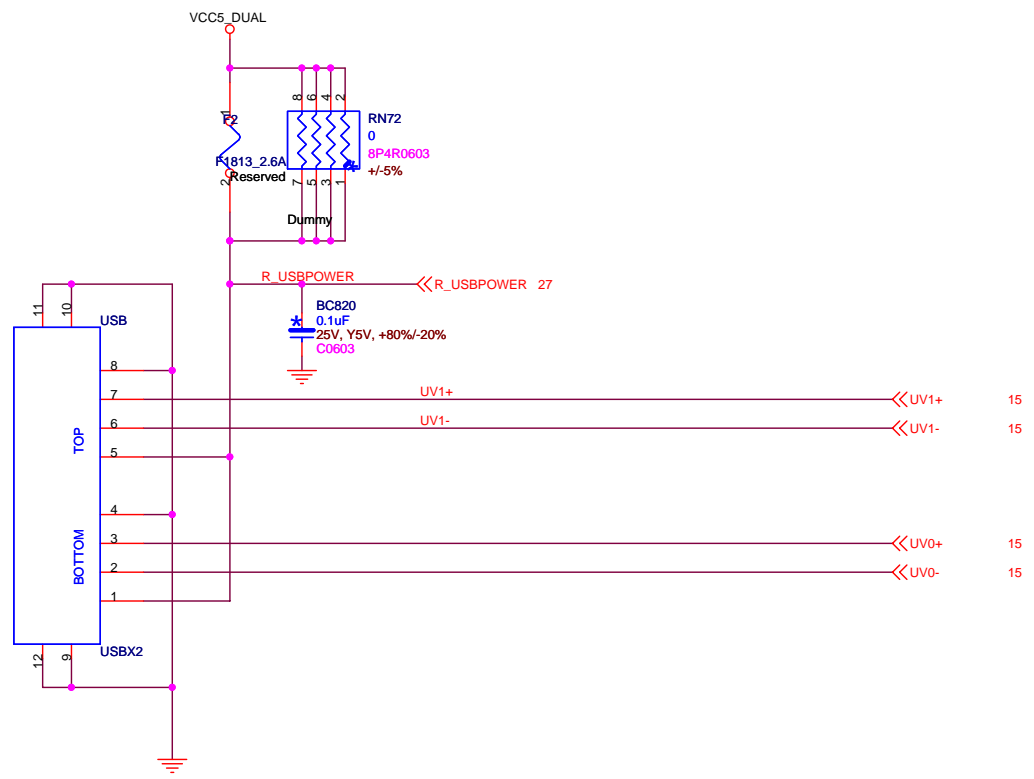


## SB3.3V





 <b>FOXCONN</b> TECHNOLOGY CORP.	
Title	
TT1394(NA)	
Document Number	Rev
661M08	A
Date: Monday, August 01, 2005	Sheet 40 of 44



- 54321
- b
- c
- B
- A
1. VRMPWD change pull up net from 3V to 12V for clock gen enable level. 7/11
2. R2488 connect to RSTSW- net for C1->C3 power on issue. 7/11
3. Stuff R2466 ,R2467 , R2468 and Pin 91 pull high 10K on ATXPG net for COM port debug. 7/15
4. to modify R805 net for HW monitor 5V. 7/18
5. Change Q80 AP15N03H as AP9916H for S3 DDR power loss. 7/5
6. Change LAN RESET from GPIO6 as GPIO9 for resume state and co-layout with PCIRESET-. R310 and R311 are switch. 7/18
7. Change R952, R954, R964, TC2 value for VR10.1 debug. 7/20
8. P31 Link WPJ 7/20
9. Add RN5 For VGMI link to 3V\_SB 7/20
10. Change BC264,BC265 to 2.2uF (BC0805)
11. Link LANRSTJ and GPIO7. 7/28
12. Add GPWAK\_ link GPIO9. 7/28

# Jumper and Header Summary

Header_1X3	Clear CMOS 1-2 : Clear CMOS 2-3 : Normal
Header_2X5_8	F_AUDIO 1 : MIC 2 : GND 3 : MIC BIAS 4 : 5V 5-6 : Line Out - R 9-10 : Line Out - L 7 : NC 8 : Key
Header_1X2	INTR
Header_1X3 (FAN3P)	SYS_FAN
Header_1X4 (FAN4P)	CPU_FAN
Header_1X4_2	SPEAKER
Header_1X4_3	SPDIF_OUT
Header_2X17_3 (FDD)	FLOPPY
Header_2X5_10	Front Panel Switch/LED 1-3 : HDD LED 2-4 : Power / Suspend LED S0 : steady green S1 : blinking S3~S5 : off 5-7 : Reset 6-8 : Power Button 9 : NC 10 : Key
Header_2X5_9	FUSB1,FUSB2
Header_2X20_20 (IDE)	PIDE
Header_2X20_20 (IDE)	SIDE



Title <b>Jumper Setting / Option Table</b>		
Size B	Document Number <b>661M08</b>	Rev A
Date: Monday, August 01, 2005	Sheet 43	of 44